CMSE 2024 Presented Developments In Power Component Standards, Sources And Reliability For Military And Space Applications

by David G. Morrison, Editor, How2Power.com

At the 27th annual Components for Military & Space Electronics Conference & Exhibition (CMSE 2024) which was held April 30-May 2nd in Los Angeles, speakers from industry gave presentations on developments in electronic components, materials and packaging for military and space applications. In keeping with the high-rel nature of the end systems, component reliability, new standards, and sourcing and supply chain issues were also featured prominently in the program.

On day one, advances in components and packaging were highlighted with special attention to heterogenous integration, which one speaker from Promex defined as "a device built using both electronic and non-electronic materials/parts" (see the reference). There were also presentations on thermal interface materials and capacitor developments. With regard to the latter, capacitors continue to be a particular focus of the CMSE program with multiple talks dealing with tantalum polymer caps and a couple addressing ceramic capacitor developments at this year's conference.

On day two of CMSE, product sourcing came to the fore. There was a panel discussion on alternate-grade parts and multiple presentations on the use of COTS components. There were also some very interesting presentations on counterfeit parts and methods for mitigation of this problem with some novel proposals such as the use of "golden samples" and "dendritic identifiers" to avoid counterfeits. In the packaging area, one speaker illustrated how this subject can be taken to a whole other level with high-rel parts in discussing the details of long-term (decades long) storage.

Overall, the conference addresses the rather broad subject matter of microelectronics as it applies to military and space systems. But within this wide-ranging area, it presented several talks on semiconductors with some focused on power semiconductors in particular.

One speaker from the aerospace industry discussed industry efforts to qualify GaN power devices for aerospace, while another offered details of his company's work in developing rad-hard MOSFETs (for which there are not many suppliers on the market.) Yet another presenter from the semiconductor industry described details and benefits of the QML-P standard for plastic packaging for space. He also noted several new power ICs from his company that comply with the standard.

Power semiconductors weren't the only power products addressed in this year's program. Another speaker from the aerospace industry described a failure analysis of a COTS power supply, which highlighted some of the challenges of using COTS products in high-rel applications and lessons learned. Meanwhile, a speaker from the magnetics industry explored a topic highly germane to power supplies when he discussed transient-induced failures in magnetics. He explained the mechanisms for these failures and ways to mitigate them. In this article, I provide highlights from these various power-oriented talks.

QML-P: A Plastic Packaging Standard For Space

In his talk, "QML-P: The Latest Standard for Radiation-Hardened, Plastic Space Packaging," Javier Valle, general manager Space Power Products at Texas Instruments, explained the benefits of plastic packaging and the QML-P packaging standard in space applications. Delving into the details of the standard, Valle described the differences in the manufacturing flows, screening procedures and conformance inspections for nonhermetic class P versus the more-established, hermetic class V (ceramic/metal can package) microcircuits.

Companies began introducing rad-tolerant and rad-hard ICs, including power parts, in plastic packages a few years ago. Renesas and TI were among the first when they presented rad-tolerant ICs in plastic packages at NSREC 2020 (See How2Power's NSREC Notes article for 2020). Since then, both companies have expanded their offerings to include both rad-tolerant and rad-hard chips in plastic packages.

Texas Instruments working with NASA and others in industry led development of the Qualified Manufacturers List Class P (QML Class P), the new standard for plastic IC packaging for space applications. As with the Class V standard for ceramic-packaged parts, the new Class P standard is intended to assure that parts will operate as intended in space environments.

TI released the following six QML-P power ICs last year:

- TPS7H4001-SP rad-hard 18-A synchronous stepdown converter
- TPS7H5001-SP rad-hard dual-output PWM controller with synchronous rectification
- TPS7H1111-SP 1.5-A rad-hard ultra-low-noise LDO
- TPS7H3302-SP rad-hard 3-A sink and source DDR-termination LDO regulator
- TPS7H2201-SP rad-hard 6-A eFuse
- TPS7H2211-SP rad-hard 3.5-A eFuse

and plans to introduce four more this year.

All of the above-mentioned parts are rad hard, therefore using the same die that would be used in the hermetically packaged parts.

The slide in Fig. 1 outlines the differences between rad-tolerant space-enhanced plastic parts and rad-hard QML-P plastic parts. These two classes of devices offer different levels of radiation protection at different price points but similar levels of electrical performance and pin compatibility. This gives designers the flexibility of using either rad-tolerant or rad-hard plastic power parts as needed for a particular project.

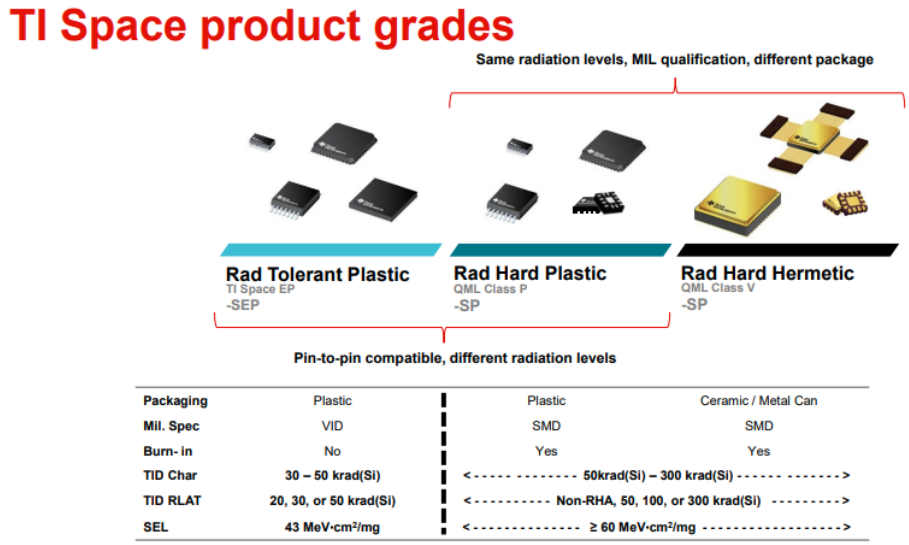


Fig. 1. TI's three classes of space-grade products offer either pin compatibility or similar levels of rad-hardness, offering designers flexibility in component selection. (Courtesy of Texas Instruments and CMSE 2024.)

Among the differences between a rad-tolerant, space-enhanced plastic part and a rad-hard QML-P plastic part, is that the latter undergoes burn-in, while the former does not. As Valle noted this is mainly due to cost, as rad-tolerant parts need to less expensive and also can tolerate a bit more risk versus parts targeting traditional space missions. However, the focus of this talk was more on the differences between QML-P plastic and QML-V hermetic parts, and the message was mostly that electrical and radiation performance is similar, but the plastic parts help address the applications' limitations in board space and weight.

As Valle observed, "the power designer has to power a monstrous FPGA and they have only a tiny area [in which] to provide a lot of power." The plastic power ICs help because they are smaller than the ceramic/metal packaged ones. Plus the plastic parts are lighter, which is another critical issue for any electronics being launched into space.

To illustrate, Valle offered a comparison of the TPS7H4001-SP synchronous stepdown converter in both ceramic and plastic as well as a similar comparison for the TPS7H1111-SP LDO (Fig. 2). In these examples, power density in terms of board space is roughly twice for the plastic parts. The plastic parts may even offer a little better efficiency due to shorter interconnect paths within the package and the shorter connections they enable on the board.

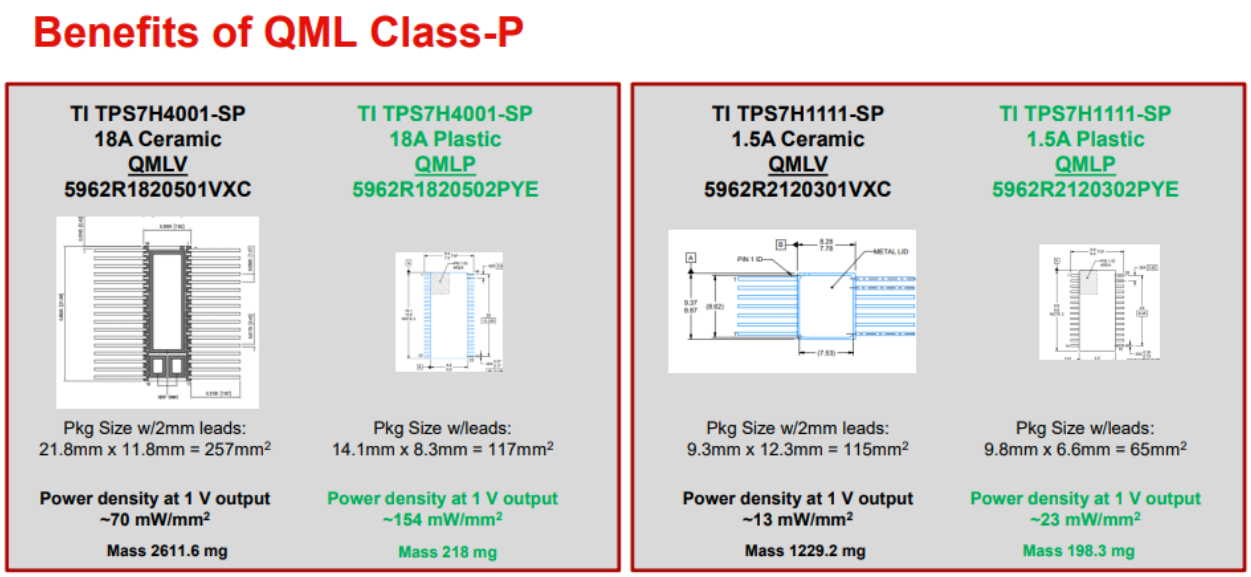
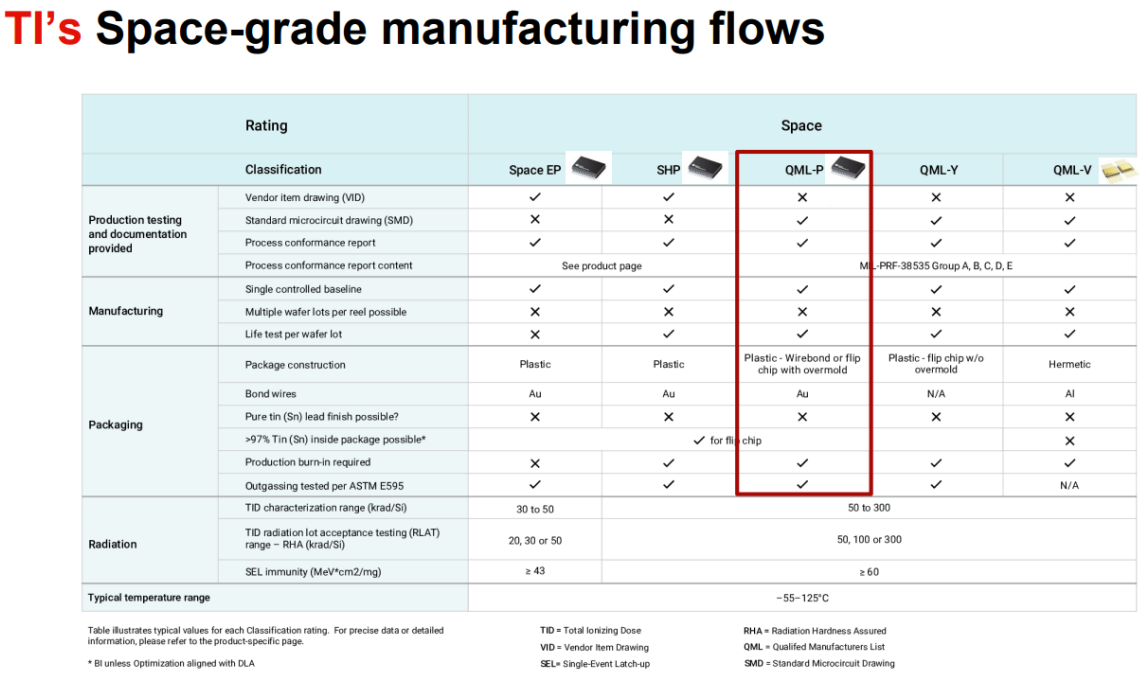


Fig. 2. Comparing the size and weight of QML-V and QML-P power components with the same funtionality. The TPS7H4001 is a synchronous stepdown converter while the TPS7H1111 is an LDO. (Courtesy of Texas Instruments and CMSE 2024.)

The introduction of space-grade components in different levels of radiation resistance and different packaging options seems to be a general industry trend as other companies like Renesas have previously announced a strategy of introducing *all* of their new space parts in both rad-tolerant and rad-hard, and plastic and hermetic packages. As Valle observed, space IC vendors "want to make sure customers have multiple options for different missions."

For those interested in the aspects of device manufacturing and screening that ensure product reliability, Valle presented slides comparing QML-P manufacturing flows and screening procedures with those of the other package types. As the slides in Figs. 3 and 4 indicate, there are some differences in these procedures.



	Rating	Space				
	Classification	Space EP	SHP	QML-P	QML-Y	QML-V
Production testing and documentation provided	Vendor item drawing (VID)	✓	✓	✕	✕	✕
	Standard microcircuit drawing (SMD)	✕	✕	✓	✓	✓
	Process conformance report	✓	✓	✓	✓	✓
	Process conformance report content	See product page		MIL-PRF-38535 Group A, B, C, D, E		
Manufacturing	Single controlled baseline	✓	✓	✓	✓	✓
	Multiple wafer lots per reel possible	✕	✕	✕	✕	✕
	Life test per wafer lot	✕	✓	✓	✓	✓
Packaging	Package construction	Plastic	Plastic	Plastic - Wirebond or flip chip with overmold	Plastic - flip chip w/o overmold	Hermetic
	Bond wires	Au	Au	Au	N/A	Al
	Pure tin (Sn) lead finish possible?	✕	✕	✕	✕	✕
	>97% Tin (Sn) inside package possible*	✓ for flip chip				✕
	Production burn-in required	✕	✓	✓	✓	✓
	Outgassing tested per ASTM E595	✓	✓	✓	✓	N/A
Radiation	TID characterization range (krad/Si)	30 to 50	50 to 300			
	TID radiation lot acceptance testing (RLAT) range – RHA (krad/Si)	20, 30 or 50	50, 100 or 300			
	SEL immunity (MeV*cm2/mg)	≥ 43	≥ 60			
Typical temperature range		−55–125°C				

Table illustrates typical values for each Classification rating. For precise data or detailed information, please refer to the product-specific page.

* BI unless Optimization aligned with DLA

TID = Total Ionizing Dose
VID = Vendor Item Drawing
SEL= Single-Event Latch-up

RHA = Radiation Hardness Assured
QML = Qualifed Manufacturers List
SMD = Standard Microcircuit Drawing

Fig. 3. Comparing manufacturing flows or TI's various space grades of parts. (Courtesy of Texas Instruments and CMSE 2024.)

Screening procedure for hermetic class V and non-hermetic class P microcircuits

Screening Tests	MIL-STD-883, test method (TM) and conditions	
	Hermetic classes	Non-hermetic classes
	Class V (class level S)	Class P (PEM) (class level S)
1. Wafer lot acceptance test	QM plan	QM plan
	TM 5007 of MIL-STD-883 (all lots)	TM 5007 of MIL-STD-883 (all lots)
2. Nondestructive bond pull (NDBP) test	TM 2023	Not part of plastic packages screening
3. Internal visual inspection	TM 2010, condition A	TM 2010, condition A
4. Temperature cycling	TM 1010, **condition C**, 10 cycles minimum	TM 1010, **condition B**, -55 to 125 °C 15 cycles minimum
5. Constant acceleration	TM 2001, condition E (minimum), Y1 orientation only	No wires in the package that can move and create shorts
6. Visual inspection	100%	100%
7. Particle Impact Noise Detection (PIND) test	TM 2020, test condition A on each device	No cavity in molded plastic packages
8. Serialization	In accordance with device specification (100%)	In accordance with device specification (100%)
9. Pre burn-in (Interim) electrical parameters test	In accordance with device specification	In accordance with device specification
10. Burn-in Test	TM 1015 240 hours at 125°C, condition D	TM 1015 240 hours at 125°C , condition D
11. Post burn-in (Interim) electrical parameters test	In accordance with device specification	In accordance with device specification
12. Reverse bias burn-in test (Static burn-in)	TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum	TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum
13. Post burn-in (Interim-reverse bias) electrical parameters test	In accordance with device specification	In accordance with device specification
14. Percent defective allowable (PDA) calculation	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)

Screening Tests	MIL-STD-883, test method (TM) and conditions	
	Hermetic classes	Non-hermetic classes
	Class V (class level S)	Class P (PEM) (class level S)
16. Seal test a. Fine leak b. Gross leak	TM 1014	Non-hermetic package, no lid to seal
17. Radiographic (X-ray)	X-ray: TM 2012	X-ray: TM 2012
18. External visual inspection	TM 2009	TM 2009
19. Qualification or quality conformance inspection / TCI test sample selection	PCR	PCR

Fig. 4. Comparing screening procedures for class V versus class P microcircuits. (Courtesy of Texas Instruments and CMSE 2024.)

For example, the screening procedure for the plastic part changes because it does not have a cavity, so there's no need for a seal test. But overall, there are no quality or reliability concerns for plastic rad-hard components, said Valle.

For more information, see the the following product pages: TPS7H4001-SP, TPS7H5001-SP, TPS7H1111-SP, TPS7H3302-SP, TPS7H2201-SP, and TPS7H2211-SP. Or contact the speaker.

Rad-Hard MOSFET Development—A New Source Emerges

In his talk, Joe Benedetto of VPT Components, gave a presentation on "VPT Component's Development of Radiation Hardened MOSFETs with LA Semiconductor". VPT Components was formed as a collaboration between VPT, a company that makes power converters and related products for space, avionics, and military applications, and SST Components, a MIL-PRF-19500 JANS-certified semiconductor manufacturer.

The origins of this business began in 2007 with the establishment of Hi Rel Components, which was then acquired in succession by Aeroflex, Cobham and MACOM. In 2018, VPT Components acquired the assets of MACOM's Hi-Rel Components business in Lawrence, MA. Since then, the company has been growing its JAN product portfolio, which includes small-signal and power bipolar transistors, SCRs, rad-hard bipolars and MOSFETs.

Meanwhile, LA Semiconductor was founded in 2021 for the purpose of acquiring the onsemi fab in Pocatello, ID. A pureplay foundry company, LA Semiconductor specializes in analog, mixed-signal and power products, and includes rad-hard process technology in its portfolio. As with VPT Components, there's a history behind the

establishment of LA Semiconductor. American Microsystems established its semiconductor manufacturing operations in Pocatello in 1971, changing its name to AMIS in 2005 when it went public.

ON Semiconductor (now known as onsemi) acquired the AMIS fabs in 2008 at which time they were producing mostly CMOS ASICs. ON Semiconductor then introduced discrete devices into the 8-inch wafer line in Pocatello. Most of these details about VPT Components and LA Semiconductor come from Benedetto's presentation, which also provides additional details on the two companies' manufacturing capabilities, certifications and standards' compliance.

However, all of those details were prelude to Benedetto's discussion of VPT Components and LA Semiconductor's rad-hard MOSFET development. As he explained, the goal of this program was to create planar MOSFETs similar to the R5 generation made by Aeroflex Rad from 2010 to 2016 at Micrel (and currently available from IR HiRel, which is part of Infineon.) To that end VPT Components "developed a custom rad-hard process flow at LA Semi and used that flow to build a rad-hard 'R5' generation power MOSFET."

In 2023, the companies developed the first device—a size 3 100-V MOSFET. The goal was for this transistor to achieve a TID rating of 100 krad(Si) and SEGR/SEB immunity at full rated drain potential using Xe with a LET of ~60 MeV-cm^2/mg and 15 MeV/n beam. These ratings were achieved. The devices also passed when subjected to Au ions with a LET of ~80 MeV-cm^2/mg and 15 MeV/n beam. However, in this case, V_{DS} was derated by 40%.

This first device is now offered as the RAD7130 MOSFET, a 100-V part with 50-mΩ $R_{DS(ON)}$—depending on the package (Figs. 5 and 6). More details on this part are shown in the slides below and extensive rad-hard test data is also included in Benedetto's presentation (which is linked to below).

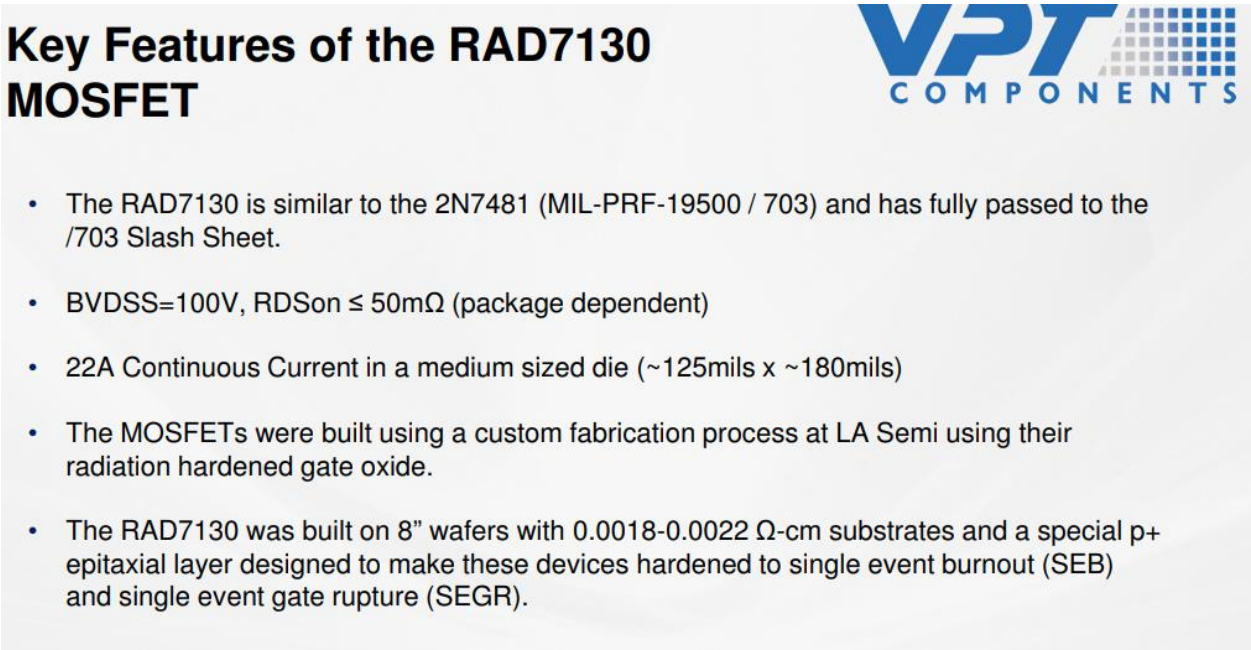


Fig. 5. The rad-hard 100-V, n-channel RAD7130 offers designers an alternative source for R5 generation planar MOSFETs. (Courtesy of VPT Components and CMSE 2024.)

Fig. 6. Key dimensions and metalization speccs for the RAD7130 planar MOSFET. (Courtesy of VPT Components and CMSE 2024.)

However, TID results for V_{TH} are also included here in Fig. 7 as Benedetto commented that this is one of the tougher specs to meet because charges get caught in the oxide layer, causing a shift in the V_{TH} voltage. But as Benedetto explained "we're able to make a good, hard oxide" which mitigates this effect.

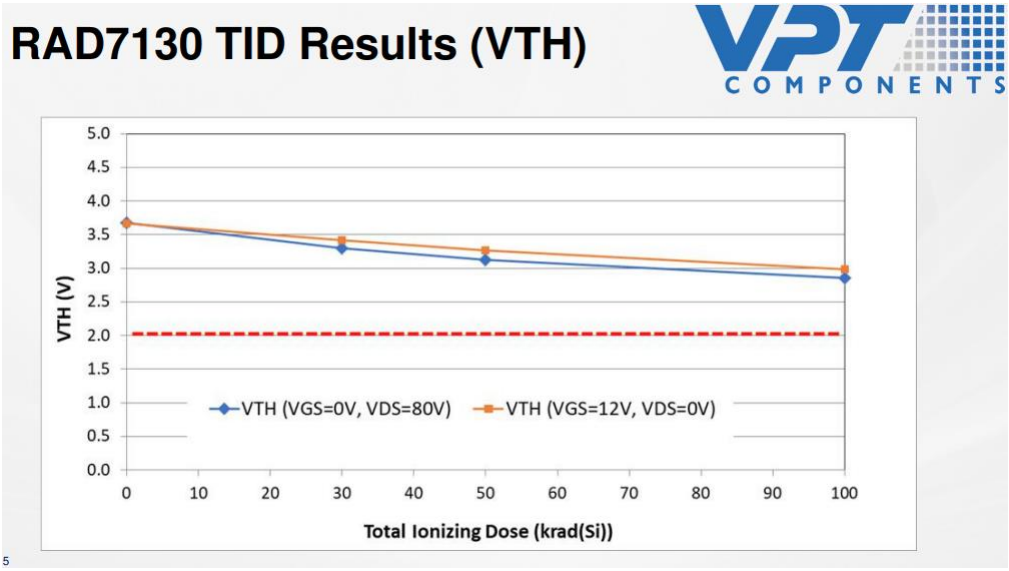


Fig. 7. Variation in threshold voltage for the RAD7130 as a function of TID. (Courtesy of VPT Components and CMSE 2024.)

In his conclusion Benedetto noted that "the TID radiation hardness was achieved using a custom radox flow applicable to higher voltage products." He also observed that "SEE hardness was achieved using a specially designed P+ epitaxial layer (designed and fabricated by LA Semi) to minimize $R_{DS(ON)}$ while withstanding SEB/SEGR." He added that LA Semiconductor is QML certified and will be MIL-STD-19500 certified through VPT components in the near future. For more information, see the presentation or email the speaker.

COTS Power Supplies—A Case Study

The use of COTS components in military and space applications was the subject of several talks at CMSE. However, one speaker discussed this issue in the context of power supplies. Aaron C. DerMarderosian, senior principal general engineer at Collins Aerospace offered a presentation on "ESS Vibration Failure of a COTS Power Supply".

As DerMarderosian observed at the start of his talk, there are multiple reasons for using COTS components in applications that might otherwise use military or space-grade parts. Cost savings, superior performance leveraging the latest technology and process advancements, and availability were three justifications that DerMarderosian cited. Other CMSE speakers echoed these points in their talks relating to COTS parts.

DerMarderosian also noted their drawbacks with respect to operation under environmental extremes including temperature, vibration, shock, humidity, salt fog and altitude. Furthermore, he cautioned about their typically short product lifecycles during which vendors "can incorporate significant changes iteratively or [replace them with] new products with little or NO notice."

With that as background, he turned to the focus of his talk, a failure investigation of a COTS ac-dc switching power supply, which had failed after being subject to transit case vibration qualification tests. The power supply was a familiar-looking, plastic-encased adapter with an IEC socket for 120- or 240-Vac input and a cord outputting its 5-V and 12-V dc supplies via a connector as pictured in Fig. 8.

Fig. 8. This ac-dc power supply with a switchable (120 or 240 V) input failed after undergoing vibration qualification tests. When the unit was partially disassembled by the customer as shown here, an issue with the ac socket was discovered. (Courtesy of Collins Aerospace and CMSE 2024.)

Upon further disassembly of the unit, as shown in Fig. 9, it was discovered that a solder joint connecting the ac line to the power supply PCB had failed. The question for the speaker's company was whether the failure was related to vibration testing since the failure was discovered after that test.

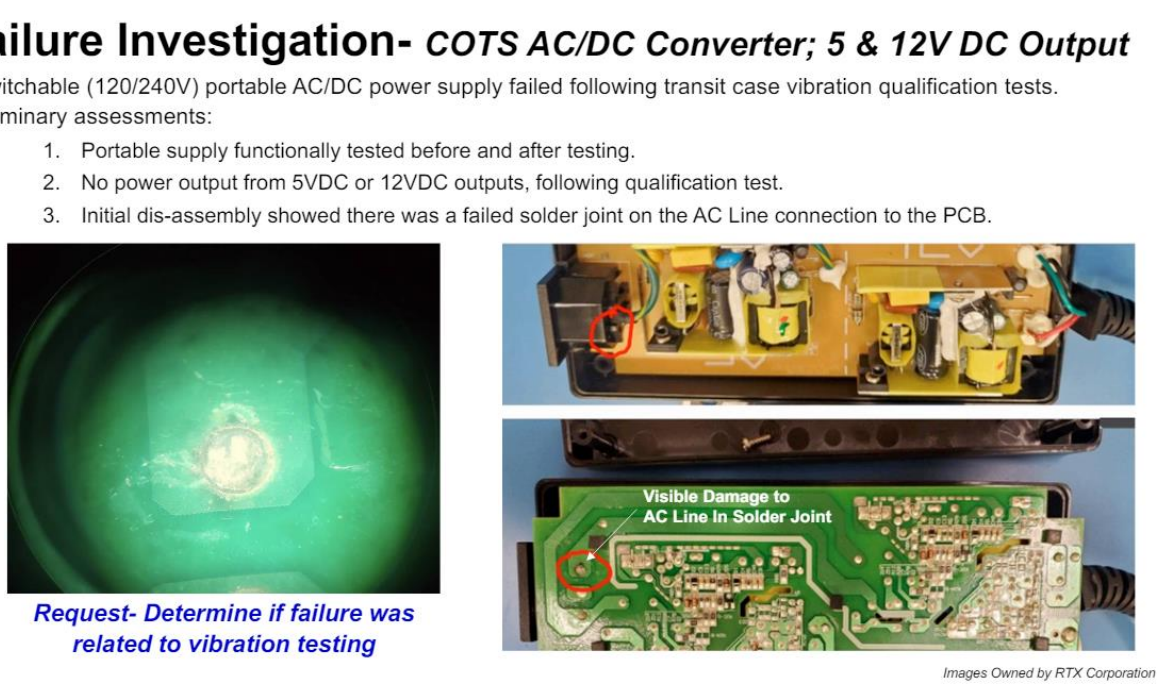


Fig. 9. Inspection of the power supply's pc board revealed a failed solder joint on the ac connection to the board was responsible for the power supply failure. But was the failure caused by the vibration testing? (Courtesy of Collins Aerospace and CMSE 2024.)

As the speaker explained, the power supply construction was simple, employing a single-layer PCB design, drilled through-holes, with all the surface-mount parts for control and logic mounted on the backside of the board. DerMarderosian observed it was very rugged in design, even while optimized for assembly cost as well as the shock and vibration as would be encountered in mobile portable device environments. But as he noted, it was only intended for operation under benign temperature conditions (0° to 70°C).

Upon inspection it was determined that the back tabs on the IEC-320 socket (the ac input receptable) did not make contact with the plastic case. This contact is necessary for mechanical stress relief when the ac cord is removed from the socket. This allowed mechanical stress to be transferred to the ac line solder joint as highlighted in Fig. 10.

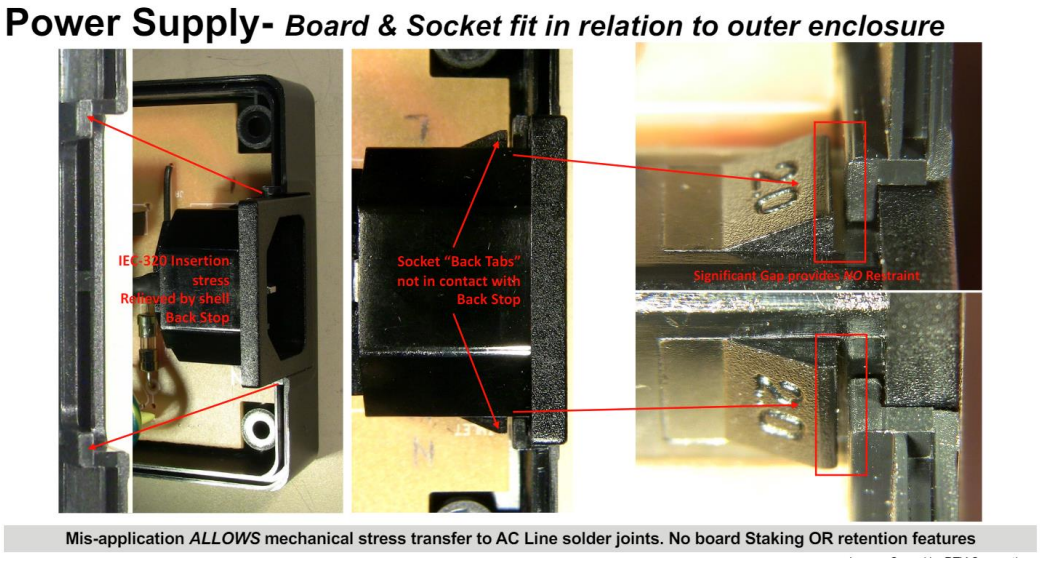


Fig. 10. An improper fit between the ac socket and the enclosure led to a lack of strain relief for the socket during removal of the power cord. (Courtesy of Collins Aerospace and CMSE 2024.)

Over multiple de-insertion cycles, the solder joint for the hot side of the line became mechanically compromised, leading to arcing and molten reflow, and ultimately an electrical failure of the joint as depicted in Fig. 11.

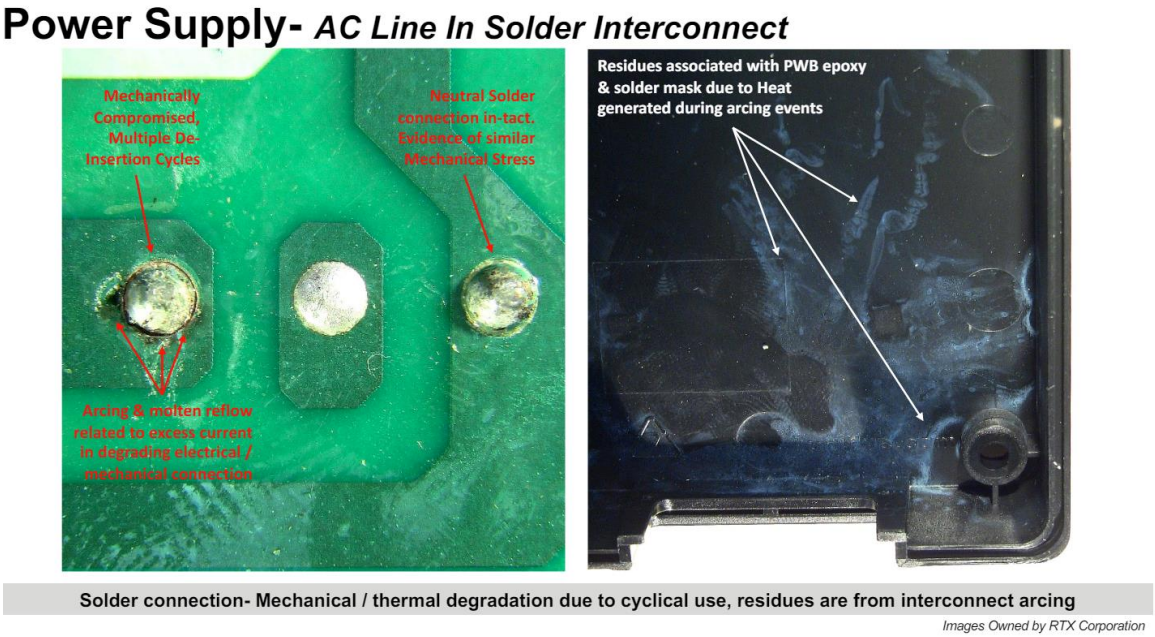


Fig. 11. Mechanical stress on the ac socket produced by multiple cycles of unplugging the ac cord damaged both solder joints where the sockets pins connect to the board, although only the hot was compromised to the point of failure. (Courtesy of Collins Aerospace and CMSE 2024.)

DerMarderosian's presentation offered further scrutiny of the failed hot connection as well as the neutral connection, which showed signs of mechanical stress but was still intact electrically. Damages to the solder joints were identified visually as photographed under magnification, then confirmed with X-rays, as shown in the speakers slides. Ultimately, it was determined that the cause of the solder joint failure was the vendor's change from one type of IEC connector to another.

As the author explained in his findings and recommendations "An alternate (available) IEC-320 socket was integrated that DOES NOT contain mating retention tabs. The alternate socket DOES contain an inner shell "back tab", but is designed for a thicker wall dimension. The tab Does NOT achieve contact with this feature to restrain the socket during power cord insertion/removal cycles." This gap between the back tab and the enclosure is identified in Fig. 10.

Explaining the specific action that caused the mechanical stress the author said, "While The IEC-320 socket applied to this enclosure provides a mechanical back-stop (insertion force), the back tab is not providing mechanical restraint, when un-plugging the ac cord."

The author concluded by explaining that prior mechanical and electrical fatigue caused the failure of the power supply, rather than the vibration test:

"Based on observations, electrical/x-ray analysis and review of the ac line input CCA design, the root cause of the failure is related to prior-use mechanical/electrical fatigue leading to ac line solder joint failure. While the ac line-in pin had continuity prior to the vibration testing, the solder joint was compromised from prior use. Lack of retention features allowed what was left of the electrical contact to open following test. In this instance, the failure is NOT a result of the vibration test."

As a final takeaway DerMarderosian advised, "If possible, use NEW assets for Qual Tests! Perform mechanical/electrical construction analyses to confirm asset viability prior to test!" For more details, see the presentation or contact the author.

Susceptibility To Transient-Induced Failures In Magnetics

Another interesting power-related talk was given by Victor Quinn, director of engineering & technology at Exxelia's U.S. Magnetics Design Center. He spoke on "Countering Threats from Transients in Magnetics".

To begin his talk he observed that "failures are often caused by latent microscopic instabilities." He noted that the "unexpected operating waveforms produced by transients" lead to concentrated stress densities, EMI, circuit malfunction, protective shutdown, and even breakdown of insulation, leading to system failure.

After noting the causes of electrical transients, he reviewed the physics underlying the response of passive components to these transients, and then related those mechanisms to the non-idealities in power transformers. The parasitic passives present in transformers lead to transient effects such as amplification, oscillation, saturation and even breakdown.

Quinn discussed several factors that make magnetic components susceptible to malfunction from transients including capacitive loading associated with high-voltage windings, nonlinearities associated with magnetization dynamics (hysteresis, nonlinear permeability, and saturation), as well as the risks associated with transient-induced saturation such as turn-on phase dependency and volt-second imbalance and transient-induced flux remanence such as reduced flux headroom for start-up or residual magnetic moment. Quinn diagrammed the effects of transient-induced eddy currents—how they increase stress densities in magnetics, resulting in higher e-fields, voltage stresses and losses.

To mitigate these effects, Quinn prescribed a series of steps that can be taken in the magnetics design stage. These include use of DFMEA techniques to identify and reduce the risks imposed by transients; carrying out experiments on magnetic component materials to evaluate their capabilities, building subassemblies on which to perform risk reduction tests and using accelerated stress tests to verify design margins (Fig. 12).

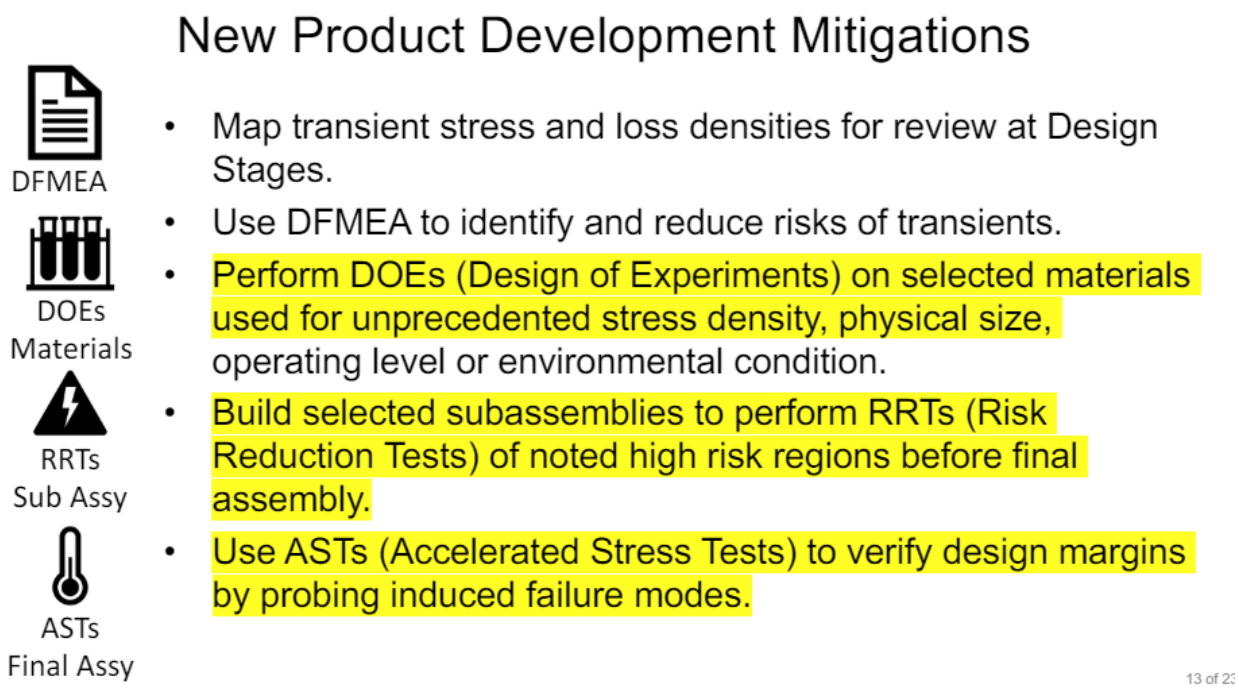


Fig. 12. A combination of analysis and testing can be performed during a magnetic component's development to lessen the likelihood of transient-induced failures during the magnetic's operation.

In subsequent slides Quinn offered specific guidance on addressing transient-induced problems in transformers such as ringing and overshoot in stepup transformers, voltage-second imbalance due to bias currents, saturation at start-up, errors in fault-current detection in current transformers, and saturating currents in pulse-forming networks. He also addressed inductor performance under transient voltage pulses and the effects of

residual magnetization on magnetorquers at turn-off. For more details, see the presentation or email the presenter.

As noted above, the power-related talks discussed in this article were part of a larger program that included presentations on other components such as capacitors, as well as packaging, reliability and sourcing topics. The full list of talks is shown in the CMSE 2024 schedule below.

CMSE 2024 Schedule

Tuesday, April 30, 2024 (Tutorials)

TUTORIAL #1 LOCATION: Los Angeles Room		
0800 - 1600	Microelectronic Component Engineering for The 2020s	**Instructors:** Ron Demcko (*Kyocera/AVX*) Trevor Devaney (*Hi-Rel Laboratories*) Jon Rhan (*Vishay*) Thomas J Green (*TJ Green Associates*)
TUTORIAL #2 LOCATION: La Jolla Room		
0900 - 1615	Heterogeneous Integration Packaging Reliability Challenges and Roadmap	**Instructor:** Richard Rao, Ph.D. *(Marvell Technology)* Co-Chair IEEE HIR Reliability TWG
1200 - 1300	**STUDENT BUFFET LUNCH** (For those attending tutorial classes) **LOCATION:** Hollywood Room	
TUTORIAL #3 LOCATION: Salon C (California Room)		
1630 - 1900	Understanding the Military Standards and Update on JEDEC and New Spec Initiatives	**Instructors:** Lawrence Harzstark (*Aerospace Corp.*) Sultan Lilani (*Integra Technologies*) Shri Agarwal (*NASA Jet Propulsion Laboratory*) Rod De Leon (*Boeing Corporation*)

Wednesday, May 1, 2024

0700	Coffee available 7AM in Annex across from Presentation Room	
0800-0815	Welcome Intro CMSE General Chair	Thomas J Green TJ Green Associates
Session #1A : Advanced Packaging Session Chair: Daniel West (*Kyocera/AVX*)		
0815-0840	Wafer Level Packaging and Reliability	Kaysar Rahim NGC
0840-0905	Introducing a Patented Ceramic Capacitor for Next Gen RF & Microwave	Scott Cooper Quantic Eulex
0905-0930	Reliability and Quality of Off-chip Interconnects in Advanced Packages in Perspective of High-Reliability Space Applications	Eric Suh NASA/JPL
0930-0955	IBM Advanced Packaging in the Northeast Corridor	Julian Warchall, Ph.D. IBM
0955-1020	COFFEE BREAK : SPONSORED BY Kyocera/AVX	
1020-1045	Reducing Board Surface Area and Improving RF Performance by Embedding Ultra-Thin Capacitors	Ryan Messina Kyocera/AVX
1045-1110	Heterogenous Integration in Complex Integrated Microelectronics Systems	Richard Otte Promex
1110-1200	**KEYNOTE: Carl E. McCants, Ph. D. (DARPA) Future Microsystems for Extreme Environments**	
1200-1355	**LUNCH in the Exhibits Area SPONSORED BY Kyocera/AVX**	
Session #1B : Thermal Considerations and Capacitor Technology Session Chair: Kaysar Rahim (NGC)		
1355-1420	Joint SAE/JEDEC Power GaN and SiC Working Group Presentation	Rod de Leon Boeing
1420-1440	Categorization, Developments, and Selection for Thermal Interface Materials	David Saums DS&A
1440-1505	Testing Methodologies and Test Systems for Thermal Interface Materials	David Saums DS&A
1505-1530	Hybrid Inspection and Assembly Process Related Challenges	Aaron Dermarderosian Collins Aerospace/RTX
1530-1550	COFFEE BREAK : SPONSORED BY Kyocera/AVX	
1550-1615	Time Dependent Capacitance Drift of X7R MLCCs Under Exposure	Brian Ward Vishay
1615-1640	Countering Threats from Transients in Magnetics	Victor Quinn Exxelia
1640-1705	The Benefits of High-Reliability in Polymer Tantalum Capacitors	Dr. James Turner Yageo/Kemet
1705-1730	High Energy, High Density Tantalum Capacitors for High Reliability Applications	Jon Rhan Vishay
1745-2000	WELCOME RECEPTION in the Exhibits Area	

Thursday, May 2, 2024

0700	Coffee available 7AM in Annex across from Presentation Room	
0800-0835	**KEYNOTE: David Beck (Space Force)** **The Critical Needs of a Resilient Industrial Base**	
	Session # 2A: COTS and Alternate Grade Parts **Session Chair: Eric Suh (NASA/JPL)**	
0835-0900	Active Packaging for Electronic Components and Assemblies	Anthony Cassanovas Honeywell
0900-0925	An Alternate COTS Approach for Space Missions	Susana Douglas NASA Goddard NEPP
0925-0950	COTS Power supply ESS Vibration failures	Aaron DerMarderosian Collins Aerospace/RTX
0950-1015	An update on non-hermetic Tantalum Polymer Capacitor Performance	Ron Demcko Kyocera/AVX
1015-1040	COFFEE BREAK : SPONSORED BY MicroCircuit Labs	
1040-1055	Lessons learned on buying commercial off the shelf products for up screening	Ben Mendoza Golden Altos
1055-1115	COTS Mission Success Improvement Workshop Results	Dr. Ryan Rairigh Lockheed
1115-1215	**Alternate Grade Parts Panel Discussion** Panelists: Pete Majewicz (NASA GSFC), Larry Harzstark (Aerospace Corp), Dr. Ryan Rairigh (Lockheed Martin Space), Mark Porter (NASA/JPL)	Moderator: Sultan Lilani Integra Technologies
1215-1330	LUNCH in the Exhibits Area	
1330-1355	Gap Analysis of COTS style EIA-364 standards to MIL-DTL-55302. What is needed and can be done for up screening Interconnects	John Riley Samtec
1335-1410	ASTM TML and TCVM methods and non-hermetics	Jayeshkumar Das, Ph.D. ORS
1410-1435	Precision Automation in Hermetic Package Sealing	Herman Itzkowitz, Rich Richardson MCL
	Session #2B : Counterfeits, Trust and Rad Hard Issues **Sesion Chair: Larry Harztark (*Aerospace Corp*)**	
1435-1500	The Numbers Crunch A Novel Approach to Transparency, Trust, and Assurance in Microelectronic Supply Chains	Richard Smith ERAI
1500-1525	Golden Samples for Counterfeit Mitigation	Lam Nguyen chipsID
1525-1550	Securing Microelectronic Supply Chains with Dendritic Identifiers	Michael N. Kozicki Densec & Arizona State University
1550-1555	COFFEE BREAK : SPONSORED BY MicroCircuit Labs	
1555-1620	VPT Component's Development of Radiation Hardened MOSFETs with LA Semiconductor	Joseph Benedetto VPT Components
1620-1645	QML-P: The latest standard for radiation-hardened, plastic space packaging	Javier Valle Texas Instruments
1645-1710	Microprocessor Reliability Enhancement Under Ionizing Radiation Using Performance Counters.	Antonio E. Teijeiro UTEP
1710-1730	**John R. Devaney Award for Best Presentation**	

Reference

"Heterogenous Integration in Complex Integrated Microelectronic Systems" by Richard Otte, Promex, CMSE 2024.