

Techniques For Safely Paralleling MOSFETs In Linear Circuits

by Jerry Steele, Red Hill Labs, Tucson, Ariz.

In power supply applications, it is common to parallel power MOSFETs to achieve current sharing and this is made easier by the positive temperature coefficient of the MOSFET's $R_{DS(ON)}$, which tends to prevent an individual MOSFET from "hogging" the current. However, this condition holds true for the case where the MOSFET is fully enhanced (in the saturation region) as it is in switching circuits, but not while the transistor is operating in the triode or linear region as it is in linear circuits.

So in switched-mode power supply applications, the inherent characteristics of the power MOSFET work in the designer's favor when paralleling power MOSFETs used as power switches in the power conversion stages but not those power MOSFETs used in circuit protection and electronics loads. In the former category, efuses and hot-swap circuits are examples where the power MOSFET operates in a linear region. This article discusses the vulnerabilities of power MOSFETs when paralleled and operated in such linear circuits, and describes techniques for ensuring current sharing in these applications.

Parallel MOSFETs: Safe Operating Area And Thermal Runaway

Paralleling power transistors is a customary method of increasing current handling capability. During the era when bipolar transistors (BJTs) were the only choice, designers learned they could parallel devices with relative ease if they accounted for certain effects.

The negative temperature coefficient of V_{BE} causes the collector current to increase with temperature (the bipolar transistor is modeled as a current source, where the MOSFET is a varying resistance). But this tendency can be controlled since the high transconductance of the bipolar transistor makes it possible to control current sharing with emitter ballast resistors. But note that thermal runaway of the entire group of paralleled bipolar transistors is still possible unless base drive temperature compensation is provided, or if they are in a current control loop.

However, with the advent of MOSFETs, the situation changed. The positive temperature coefficient of the MOSFET's $R_{DS(ON)}$, as shown in Fig. 1, means that an individual device will tend to limit its own drain current. But this requires that the MOSFETs have a gate drive that fully enhances them, such that they are operating in a purely resistive region as is the case in a switched circuit. Unfortunately, that's not the situation when MOSFETs are operating in their triode or linear region as they are in a linear circuit.

So that's one problem when paralleling power MOSFETs in linear circuits. A second difficulty arises from the temperature coefficient of V_{GS} as shown in Fig. 2. While most MOSFETs exhibit a region of negative tempco of drain current versus gate voltage as shown by the green arrow, this region only occurs at current levels too high to be useful. A large portion of the curve exhibits a positive TC of drain current as shown by the red arrow, which prevents proper current sharing and can result in thermal runaway of one or more parallel MOSFETs.

Linear circuits in which power MOSFETs may be paralleled fall into three basic categories:

1. Simple parallel configurations of MOSFETs, which are discouraged;
2. eFuse, or switching-type protective circuits that are normally fully enhanced but can go into current-limiting turn-on and protective modes that require linear operation of one or more parallel MOSFETs;
3. Electronic loads and linear power amplifiers, where the MOSFETs are always in a linear region.

It should be noted that this article will focus on the linear and thermal considerations for paralleling MOSFETs. It is also generally recommended to add series gate resistors (with typical values between 10 and 100 Ω) to prevent parasitic oscillations in MOSFETs.

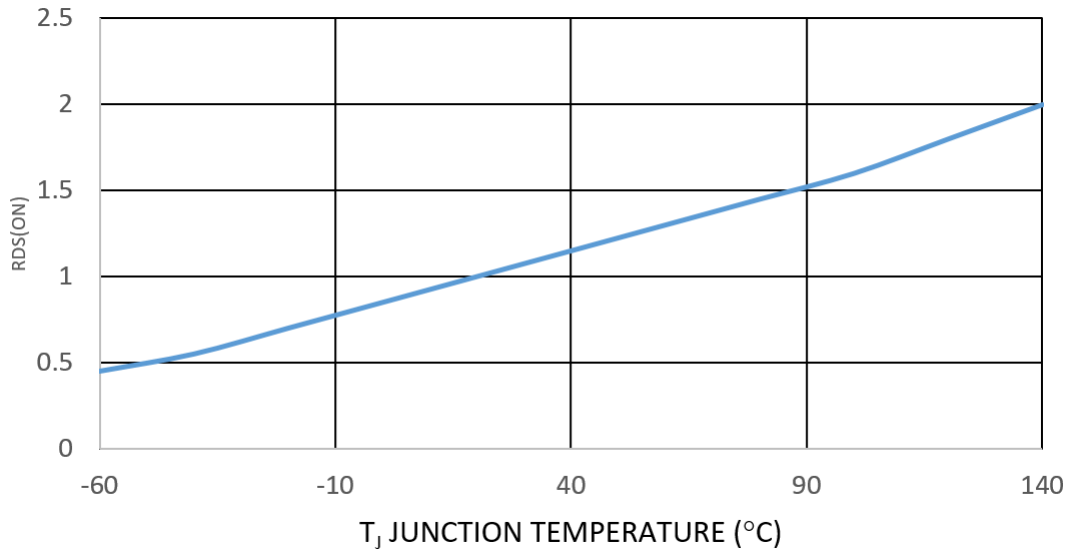


Fig. 1. A MOSFET's $R_{DS(ON)}$ exhibits a positive tempco.

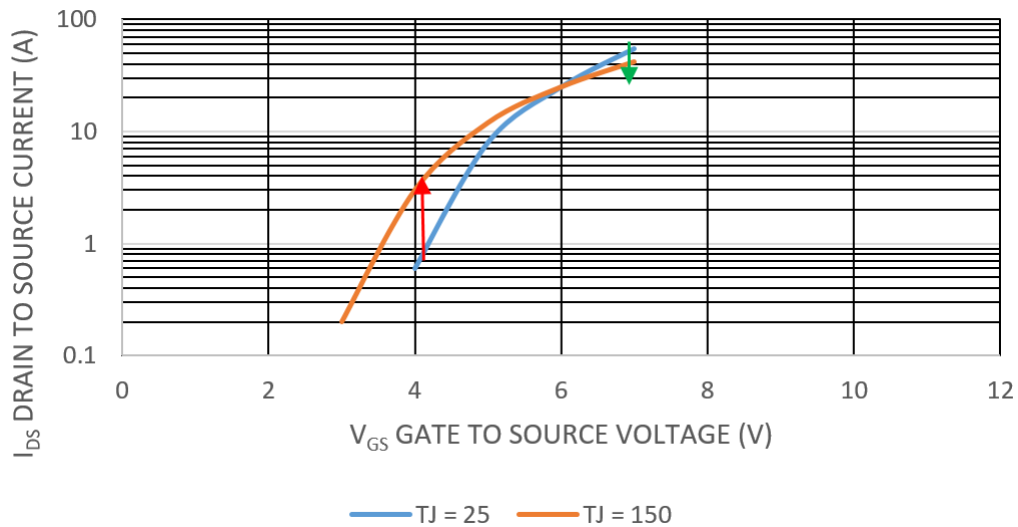


Fig. 2. MOSFET V_{GS} vs temperature.

eFuse And Current Limiting Switch Circuits

The devices referred to as eFuses perform a nearly identical function to those referred to as hot-swap controllers, and both types of devices are subjected to switching and linear modes of operation. They can be completely off or fully enhanced, or in a linear protective mode when needed. It should be noted that there are eFuse applications having only modes of totally off or totally on (switching), and such applications support a reliable implementation of parallel MOSFETs. But where that is not the case, additional steps must be taken to ensure current sharing.

eFuse and hot-swap controllers typically provide the current sensing and gate drive for the MOSFET protection control loop. Many controllers have a single current sense as well as a single gate drive. With this type of controller it is possible to parallel MOSFETs if you consider that when the loop is controlling current it will drive the gate voltage down to the current limit value. So, if either MOSFET attempts to "hog" current, the loop is

essentially controlling the highest current MOSFET and the companion MOSFETs may be conducting little or no current.

This situation in itself is not harmful or destructive but it requires the designer to treat the MOSFET pair as if they had the SOA of a single MOSFET. As a rule, anytime more than one MOSFET is driven from a single gate line (or more exactly, a single current control loop) you are limited to the SOA of a single MOSFET (although you do have the advantage of lower $R_{DS(ON)}$ when the MOSFETs are fully on).

An improvement is offered by some recently developed controllers that provide separate current sensing and gate drive for each MOSFET. This maximizes the performance of the MOSFETs since you have the full SOA available from the pair (or however many devices for which the controller has dedicated channels).

The LTC4282, depicted in Fig. 3, is an example of such a controller. As will be seen, the concepts used in the LTC4282 are applicable to paralleling MOSFETs in any linear circuit to provide the full SOA of multiple MOSFETs. The idea is that you have to parallel control circuits, not just the MOSFETs.

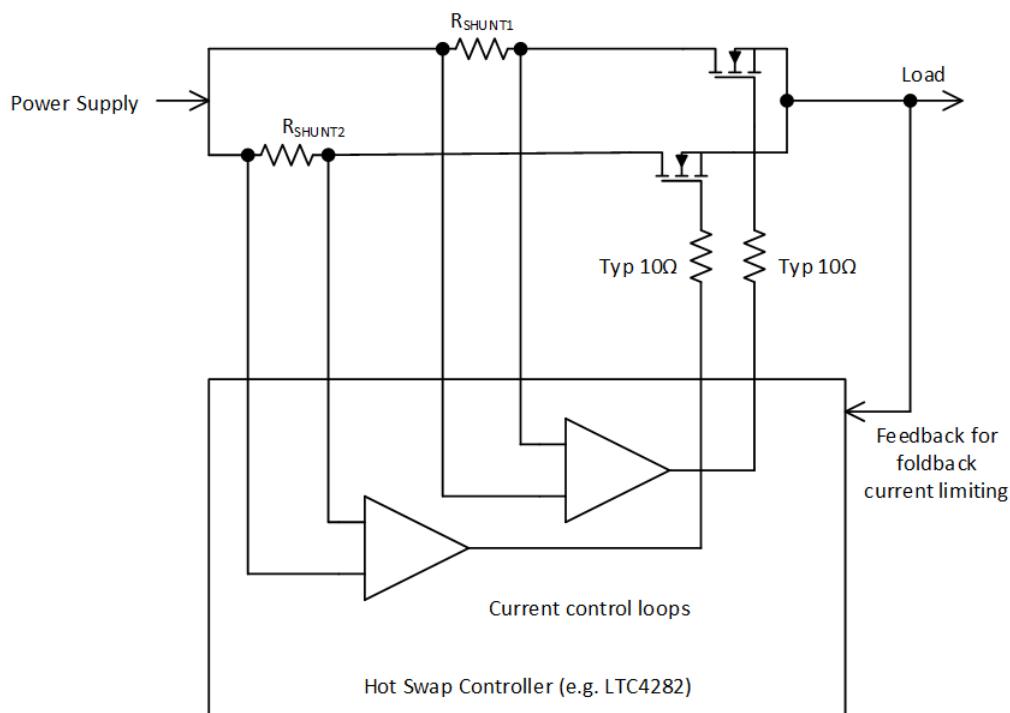


Fig. 3. An example of a hot-swap controller designed to drive parallel MOSFETs and achieve the full SOA of each transistor.

Designing Linear Circuits With Parallel MOSFETs

For many years, electronic loads (such as those from Chroma Systems Solutions and Kikusui) have shown the way to reliably parallel MOSFETs. The basic building block of the electronic load consists of the op amp and MOSFET current source as shown in Fig. 4.

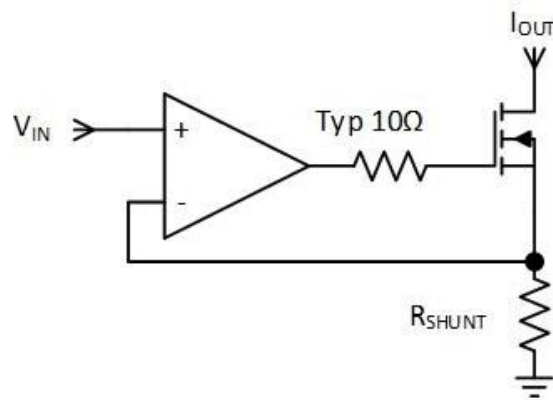


Fig. 4. A simplified schematic for an electronic load channel.

The operation of this familiar and simple circuit is very intuitive. V_{IN} is a voltage to program the desired current with the actual current value determined as a function of V_{IN} and the shunt resistor value with a simple equation shown here that applies to both Figs. 3 and 4:

$$I_{OUT} = \frac{V_{IN}}{R_{SHUNT}}$$

Commercially available electronic loads use a bank of these current source circuits in parallel to provide their high current, power, and SOA capability. While the basic circuit is a current source, the load boxes can have global control loops to make them constant current, constant voltage, resistive, and even reactive. But what's significant for this discussion is that these load boxes reliably parallel a large number of MOSFET circuits, not just MOSFETs.

Linear power amplifiers have been available in the past that paralleled MOSFETs with nothing more than source pin "ballast" resistors. But for the highest possible reliability even a power amplifier should be utilizing a closed-loop current-control circuit. Bandwidths up to the hundreds of kilohertz are practical with this configuration, while wider bandwidths can be difficult to design and compensate.

For a linear power amplifier or bidirectional electronic load, a drain output topology with floating load power supplies is readily configured as a current source output circuit as shown in Fig. 5. A voltage source output is provided by adding an extra amplifier at the input with global feedback from the load. The local MOSFET circuits provide control of quiescent bias over temperature as well as current sharing. The current control performance of the circuit improves with higher-value source resistors, and low op amp offset provides tighter quiescent biasing.

Note that this MOSFET circuit configuration results in the MOSFETs having voltage gain as well as bandwidth and phase shift considerations when used with a global loop. An advantage of this configuration is that the driving op amps can operate on the customary lower-voltage op amp power supplies (e.g. ± 15 V) while the output stage is capable of providing voltage gain along with higher output voltages limited only by the MOSFET voltage ratings and the power supplies used on the output stage.

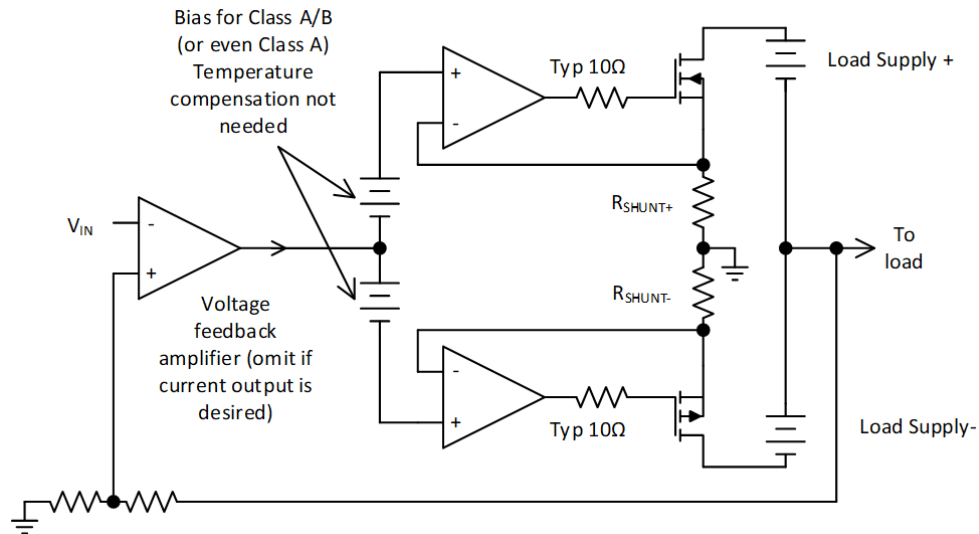


Fig. 5. This linear-voltage-output power amplifier topology uses current control loops for each MOSFET and has a global voltage feedback loop.

A method of paralleling MOSFETs based on the circuit in Fig. 5 is shown in Fig. 6. Notice the straightforward connection of the inputs and outputs for the individual current sources.

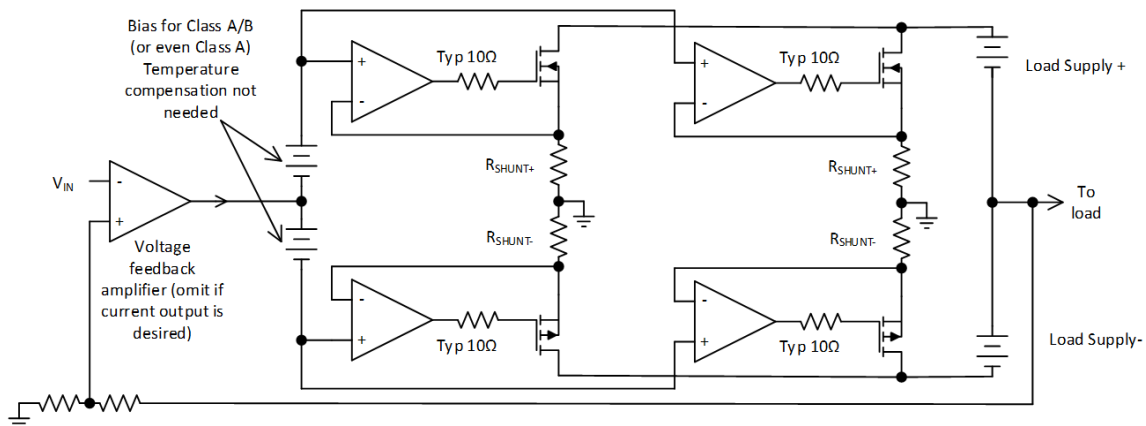


Fig. 6. A linear power amplifier with individually current-controlled parallel MOSFETs.

The Hybrid Microcircuit Option

In the event your system can be built as a hybrid microcircuit there is one other, esoteric option. In this case you can purchase your MOSFETs in die form with the possibility that the MOSFET manufacturers can ensure that you get "adjacent die" in your MOSFET die wafer pack. Adjacent die are those which were side-by-side on the semiconductor wafer before it was diced and therefore have nearly identical characteristics. This is as close as you can get to true MOSFET matching.

This method was used successfully in the early 1990s by Apex Microtechnology in high-power linear amplifiers that have proven to be rugged and reliable. An example is the Apex PA05 shown in Fig. 7.

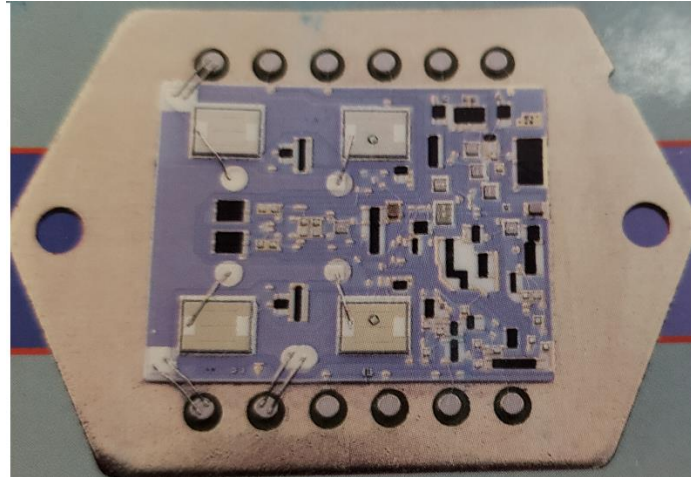


Fig. 7. The Apex PA05 power op amp shows paralleling of adjacent-die MOSFETs. Also note the small-signal bipolar transistor die attached atop the inner MOSFETs to implement thermal limiting.

Conclusion

In summary, attempting to parallel discrete MOSFETs directly, even including source ballast resistors, provides questionable long-term reliability at best. With this approach, it's very challenging to guarantee reliability over extremes of supply voltages, operating temperatures, and load conditions. The adjacent die solution, with its near-ideal MOSFET matching, has been proven in production but is difficult and expensive to implement.

Fortunately, modern operational amplifiers are small, economical, and offer the performance that eases the design of a circuit that makes it possible to parallel MOSFETs safely. ICs such as hot swap controllers, eFuses, and load boxes validate the circuit approach to paralleling MOSFETs.

Lastly, it's generally worthwhile to seek out the largest MOSFET possible, as it may satisfy your requirements without paralleling devices. MOSFETs such as the IXYS IXA60IF1200NA, rated at 88 A and 1200 V, may meet your high current requirement with a single device. Many of these large MOSFETs are found in SOT-227 packages as shown in Fig. 8.



Fig. 8. Large MOSFETs are available such as this IXYS IXA60IF1200NA in a SOT-227 package which may provide the required power without the need to parallel.

References

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3. "What are the considerations when using MOSFETs in parallel?" Toshiba FAQ.

4. "MOSFET Paralleling (Parasitic Oscillation between Parallel Power MOSFETs)," Toshiba application note, 07-26-2018.

About The Author



Jerry Steele has a long association with power management products from his early days at Burr-Brown, Apex Microtechnology, National Semiconductor, Maxim, and at Texas Instruments as a senior member of technical staff. His experience has covered a variety of products including precision analog and mixed-signal devices dedicated to temperature, current, and power measurement to system management and protection devices including devices such as eFuses and hot swap controllers. Jerry has authored a considerable number of analog and mixed-signal articles over the years, and co-authored five patents.

For further reading on circuit protection and hot swapping in power supply designs, see the How2Power [Design Guide](#), locate the Design Area category and select "Power Protection."