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ZVS Flyback Architecture Enables 70-W Output For AC-DC Converters Without PFC

Eggtronic has unveiled a new addition to its QuarEgg ZVS flyback family of high-density power conversion solutions with an ultra-high-efficiency architecture that increases the power output available to designers before they are required to implement power factor correction (PFC). Built around Eggtronic's forced zero voltage switching (ZVS) flyback architecture, the 70-W version of QuarEgg delivers peak efficiencies of 94.5% and above average efficiencies (see Fig. 1) that are significantly higher than the competition across the load range, according to the vendor.

This performance also represents an improvement in efficiency versus the previously announced QuarEgg architecture. This was achieved through a change in the control algorithm implemented in a new secondary-side controller IC, the EPIC2ACQxx. As before, this chip is a mixed-signal, low-power controller with multi-mode operation and synchronous rectification control that provides all the necessary primary-side regulation without the need for an optocoupler. This 5-mm x 5-mm device incorporates an optimized low-power mode for enhancing performance at zero and light loads and provides built-in protection against overvoltage, overcurrent, brownout and extreme temperatures.

European standard EN61000-3-2 dictates that PFC is required for any power supply rated above 75 W. This has resulted in a market that is dominated by 65-W ac-dc converters to ensure that less than 75 W is consumed from the mains input to avoid the PFC requirement. With this new version of QuarEgg, engineers can develop ac-dc converter solutions with 70-W output capability, making non-PFC designs available to applications that might previously have required power factor correction.

Using the new QuarEgg architecture, designers can significantly reduce total operational losses when compared to conventional active clamp flyback (ACF) and quasi-resonant (QR) topologies, simplify overall circuit design and thermal management and reduce component count, form factor and cost, according to the vendor.

The new QuarEgg architecture also provides component and cost reductions versus the earlier version of this architecture. Use of the new EPIC2ACQxx controller enables cost-saving component reductions on the secondary side, while a new startup IC provides cost savings on the primary side versus the previous QuarEgg design.

Specifically, the older design employed a primary-side aux start-up IC + gate driver for the primary-side MOSFET, and that IC cost approximately $0.30 to $0.50. That chip was replaced by Eggtronic's EPIC1Axxx IC in the new QuarEgg design, and this IC costs <$0.10. So $0.20 to $0.40 has been saved off the BOM from these primary-side changes.

Meanwhile, on the secondary side, the older QuarEgg design employed an aux buck circuit which cost about $0.10 to $0.20. In the new design, this has been replaced with a self-driven aux buck circuit controlled by the EPIC2ACQxx and this new aux buck costs only about $0.05. This results in a savings of about $0.05 to $0.15 off the BOM. These reductions in parts count and BOM costs are depicted in Fig. 2.

Eggtronic has built a demonstration of the QuarEgg technology that provides 70-W output in a form factor of just 72.6 mm x 39.1 mm x 17.5 mm. Smaller form factors will be possible using the architecture and target applications will include chargers for portable equipment, set-top boxes, routers and Bluetooth speakers, IoT and small consumer devices, and high-brightness LED lamps.

"Integrating PFC into a design increases complexity, component count and size, three things that OEMs look to minimize wherever possible," says Igor Spinella, Eggtronic's CEO and founder. "To date, designers have had to choose 65-W technologies and sacrifice efficiency for cost with QR topologies or spend more to obtain the higher efficiencies of ACF. Now, by creating a 70-W version of our proven QuarEgg forced ZVS ac-dc architecture, we are opening up the possibility of PFC-free designs to higher powers than previously possible using the best ACF architectures, with smaller form factors and at costs that are comparable with QR alternatives."

For more information, contact the company.

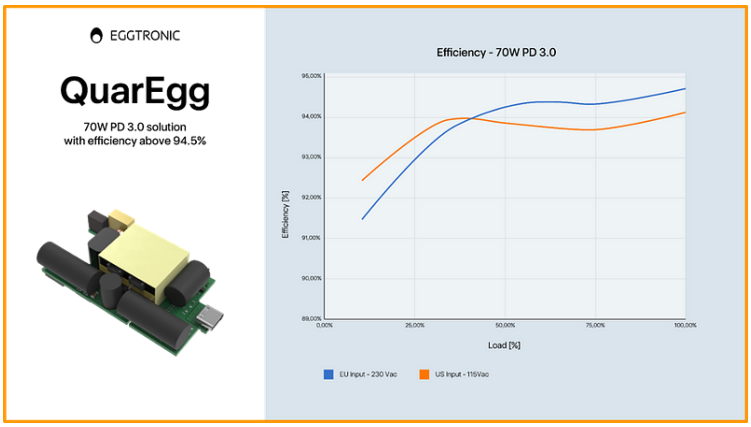

Fig. 1. The EN61000-3-2 European standard dictates that PFC is required for any power supply rated above 75 W. This has resulted in a market that is dominated by 65-W ac-dc converters to ensure less than 75 W is consumed from the mains input. Now, with the latest evolution of Eggtronic's QuarEgg ZVS flyback architecture, engineers can develop solutions that support 70 W, making non-PFC designs available to applications that might previously have required power factor correction.

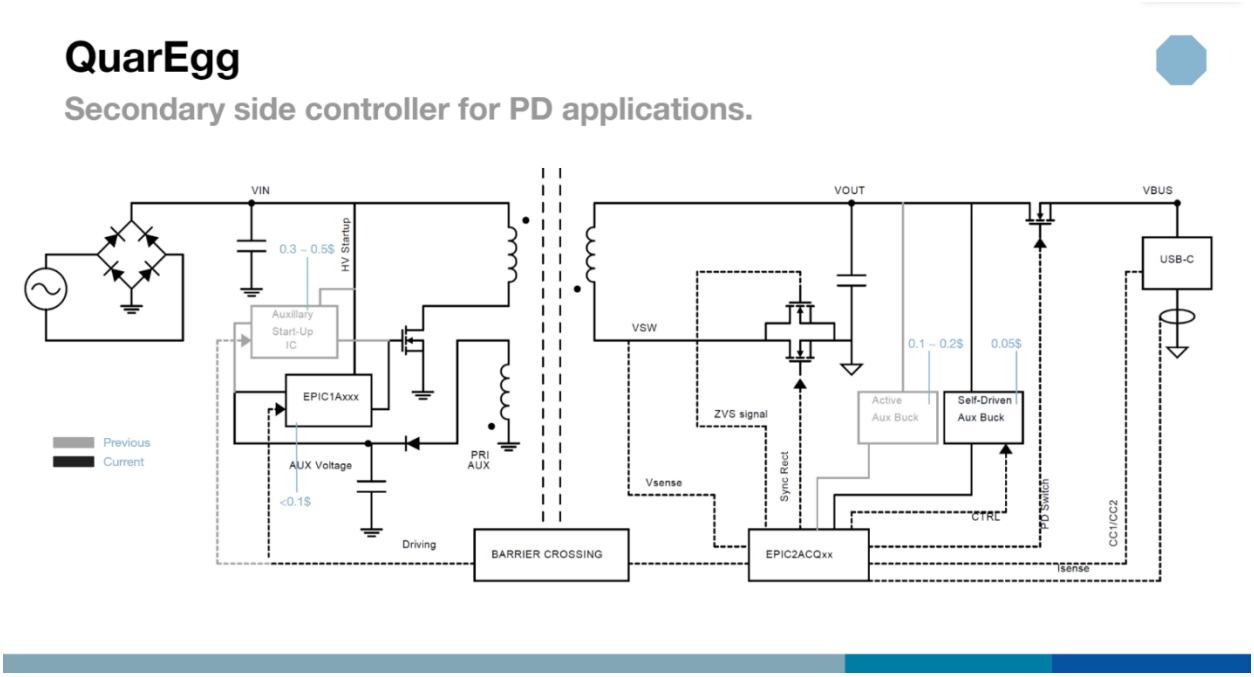

Fig. 2. A new version of Eggtronics QuarEgg ZVS flyback architecture achieves higher efficiency through the use of an improved control algorithm in a new secondary-side controller IC, the EPIC2ACQxx. This controller also enables replacement of an active aux buck circuit with a self-driven aux buck, lowering BOM cost. Even higher savings are achieved on the primary side through replacement of an aux start-up IC + gate driver with the new EPIC1Axxx IC.