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Characterizing Dynamic C_{OSS} Losses In 600-V GaN HEMTs

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Power semiconductor devices are used to control high current or power in a wide range of systems such as power converters, inverters, and switched-mode power supplies. To maximize the efficiency of such systems, power device losses must be minimized. Soft switching or zero voltage switching can eliminate or dramatically reduce turn-on losses, but there are still losses that need to be considered, including those originating from the device output parasitic capacitance C_{OSS}, referred to as C_{OSS} losses or dynamic C_{OSS} losses.

Every time a power device is switched, its output parasitic capacitance C_{OSS} incurs a loss because it is charged and discharged. C_{OSS} losses, then, are proportional to the switching frequency. These losses occur no matter what semiconductor material the power device is made of. However, because GaN enables higher-frequency operation, C_{OSS} is more of a consideration for GaN power HEMTs than MOSFETs made from other materials, such as silicon (Si) or silicon carbide (SiC).

One challenge for engineers is that C_{OSS} losses are not easy to characterize. Furthermore, the industry and the scientific community still lack a solid understanding of the underlying physics mechanism. This article will explore different methods for characterizing C_{OSS} losses—nonlinear resonance, Sawyer-Tower, and calorimetric.

After explaining the advantages of the calorimetric characterization method, it will present a novel addition to this method that simplifies setup calibration and speeds C_{OSS} loss characterization by eliminating the need to wait until the thermal system has reached thermal equilibrium. Finally, it will show how C_{OSS} losses are dependent upon slew rate (dV_{DS}/dt), displacement current (I_{COSS}), switching frequency (f_{sw}), and drain-source on-resistance ($R_{DS(ON)}$).

Characterization Methods

Several characterization methods have been proposed to measure C_{OSS} losses, most commonly: nonlinear resonance,[1,2] Sawyer-Tower,[3] and calorimetric.[4,5]

Nonlinear resonance characterization is based on electrical measurements. This method is attractive because it is simple, fast, and does not require preventive calibration of the measurement setup and testbench. Unfortunately, this characterization method does not match how power devices are typically used in typical power electronics applications, namely switching current on and off under high-voltage conditions as in a classic half-bridge or full-bridge configuration normally used in common power conversion systems.

Characterization based on a Sawyer-Tower circuit is a known and established method that has been explored and exploited in the scientific and industrial communities. However, much like nonlinear resonance characterization, the methodology does not match how MOSFETs are used in the usual power electronics applications.

That's because the device under test is subjected to a sinusoidal voltage variation at its drain and source terminal, which does not match the common square-wave voltage swing resulting from common power electronics circuits (such as half-bridge or full-bridge) operation. Moreover, the method also does not support the variation of V_{max}, f_{sw}, and slew rate independently, which makes matching specific combinations of operating parameters more difficult to set during characterization.

Accurate And Simple Calorimetric Characterization Of C_{OSS} Loss

C_{OSS} loss characterization based on calorimetric methodology was originally developed and proposed by ETH Zurich University. While it has the disadvantage of being more complex to set up than either the nonlinear resonance or Sawyer-Tower characterization methods, this is part of what enables its key benefit. That is, it permits C_{OSS} characterization measurements while the DUT works under voltage conditions which closely

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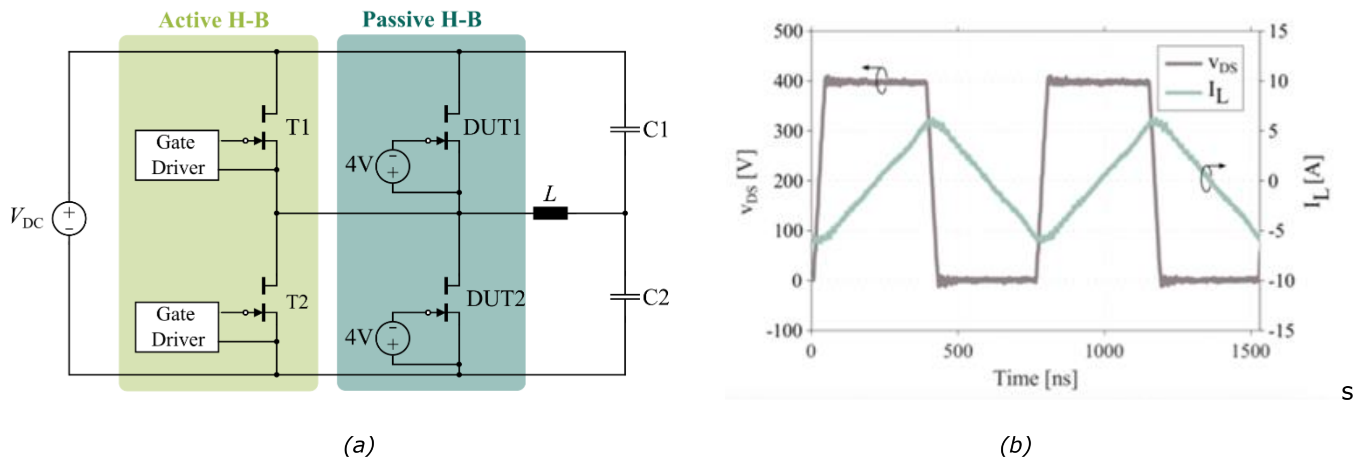
resemble the ones observable during power device operation in typical power electronics applications, namely V_{DS} square waves.

Fig. 1 shows the test circuit used to characterize power MOSFET C_{OSS} losses across a range of voltage, current, switching frequency, and slew-rate conditions. The test circuit utilizes an active half bridge and a passive half bridge connected to an LC resonant tank. Power GaN transistors T1 and T2 operate with a 50% duty cycle and modulate the resonant current through the LC-tank and, at the same time, the C_{OSS} charging and discharging (displacement) current of the GaN HEMTs DUT1 and DUT2 comprising the passive half bridge. V_{DS} is the voltage across either DUT1 or DUT2 (depending on the convention chosen for the tank current direction in the waveforms depicted in Fig. 1).



(a) (b)

Fig. 1. Test circuit schematic (a) and waveforms (b) for calorimetric characterization of C_{OSS} loss.

What is of interest here is that the GaN devices comprising the passive half bridge experience only dynamic C_{OSS} losses as they are always in the off-state during operation of the active half bridge. This is obtained by setting their gate-source bias to -4 V (as illustrated in Fig. 1). In addition, by adjusting dV_{DS}/dt through tank inductance (L), and switching frequency, the DUT can be characterized across a spectrum of operating conditions relevant to a specific system or application.

Measurements are made by connecting the active and passive half bridges to two different heat sinks. Look-through holes in the test PCB allow the temperatures of components, namely DUT1 and DUT2, T1 and T2, and $HS_{passive}$ and HS_{active}, to be measured with an infrared (IR) camera (see Figs. 2 and 3).

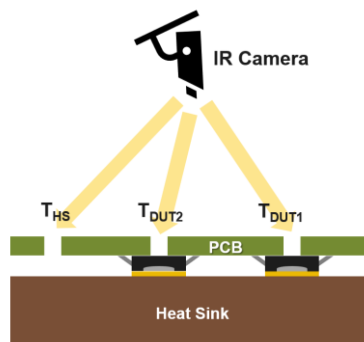


Fig. 2. Calorimetric characterization measurements are made using an IR camera. Temperatures of the GaN HEMTs (backside of their packages) and of the heat sink are measured via look-through holes realized across the PCB.

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Fig. 3. The temperatures of all six components of interest are measured during operation of the active half bridge (T1 and T2) to determine the C_{OSS} losses associated with the passive bridge (DUT1 and DUT2).

Calorimetric Calibration

Before C_{OSS} loss measurements can be made, the characterization system requires a thermal calibration. The calibration process involves exciting a device of the test circuit, for example DUT1, with several values of constant power dissipation. Temperatures are measured for all six observation points to assess the heat-up effect across all the other components over time. The process is then repeated, one at a time, for the other three GaN HEMTs of the circuit (i.e. DUT2, T1 and T2).

Measuring over different power and temperature values results in the matrix K_{th}:

$$K_{th} = P_{calibation} \cdot T^{+}_{calibration}$$

where K_{th} is a matrix describing the thermal conductances of the system, including all thermal cross-couplings of the four GaN devices; $P_{calibation}$ is the matrix of the calibration powers; $T_{calibration}$ is the matrix of the temperatures of all the components in the system recorded during the calibration procedure; and $T^{+}_{calibration}$ is the Moore-Penrose pseudo-inverse matrix of $T_{calibration}$.

The thermal conductance matrix K_{th} captures the relationship between powers and temperatures within the thermal system. It also accounts for all thermal cross-coupling between the four GaN HEMTs of the circuit.

Typically, temperature measurements would need to be taken after the thermal system had finally reached the steady-state condition, i.e. thermal equilibrium. However, waiting for such a thermal system to achieve a steady state can take more than an hour in some cases.

With the proposed calibration approach there is no need to wait for the system to reach the thermal equilibrium. Fig. 4 shows, for example, the temperature rise of the HEMT DUT1 while it is subjected to a 5-W constant power dissipation. It can be seen that after about 20 seconds, the temperature difference (ΔT) between DUT1 and its corresponding heat sink (passive heat sink) is constant.

In other words, after 20 seconds, the only change in DUT1 temperature is dictated by the (thermal) charging of the passive heat sink thermal capacitance, and ΔT remains unchanged even when the system has finally reached the thermal equilibrium. Thus, accurate measurements can be made after less than a minute.

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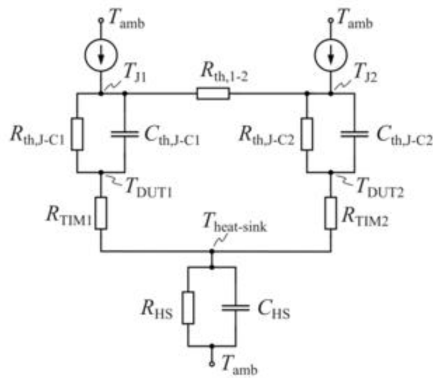

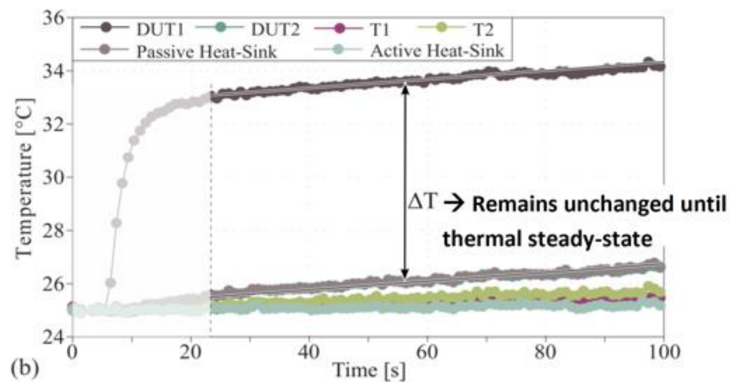

Fig. 4. After about 20 seconds, the temperature difference ΔT between the device under test (DUT1 in this case) and its heat sink is essentially constant.

Measuring C_{OSS} Losses

After calibration and computation of the thermal conductance matrix K_{th}, C_{OSS} losses can be measured for the two GaN DUTs of the passive half bridge while they are subjected to a drain-to-source square wave characterized by the desired frequency and V_{DS} slew rate. The losses generated by the two HEMTs (DUT1 and DUT2) can be obtained directly by using their measured temperature increase with respect to the measured temperature of the passive half-bridge heat sink in combination with the previously determined thermal conductance matrix K_{th}.

For example, Fig. 5 shows calibrated C_{OSS} losses obtained experimentally for various frequency values and slew rates (dV_{DS}/dt) with the commercially available Infineon CoolGaN IGOT60R070D1, i.e. a 600-V GaN HEMT featuring 55-mΩ on-state resistance. This graph shows what the losses are and their dependency upon slew rate and switching frequency.

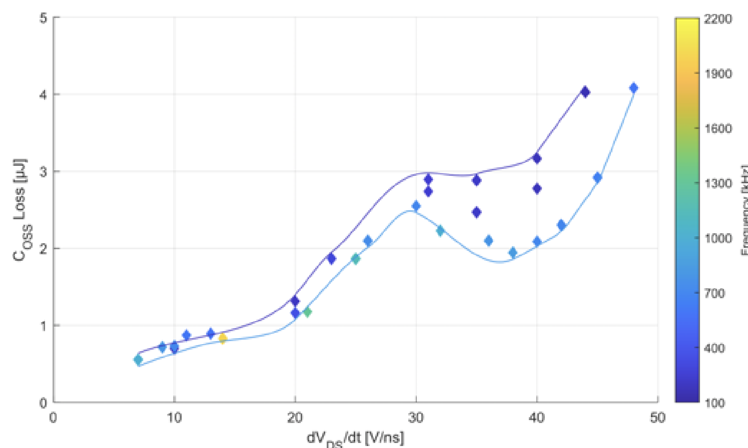

Fig. 5. Calibrated C_{OSS} losses obtained with the Infineon 55-mΩ, 600-V CoolGaN HEMT and their dependency upon V_{DS} frequency and slew rate.

Fig. 6 shows C_{OSS} losses for two other commercially available Infineon CoolGaN HEMTs featuring two different values of $R_{DS(ON)}$, i.e. 55 mΩ (IGOT60R070D1) and 37 mΩ (IGOT60R042D1). As can be seen in the graph on the left, the device with the larger chip area (smaller $R_{DS(ON)}$) shows larger C_{OSS} losses and larger loss dependency upon the frequency than its smaller-area (larger-$R_{DS(ON)}$) HEMT counterpart. The graph on the right shows the C_{OSS} loss dependency as a function of the equivalent displacement current I_{Coss}, which can be

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calculated from the knowledge of dV_{DS}/dt and Q_{OSS} values at a specific voltage (400 V in this case), whereas Q_{OSS} values can be retrieved for both HEMTs from their datasheets.

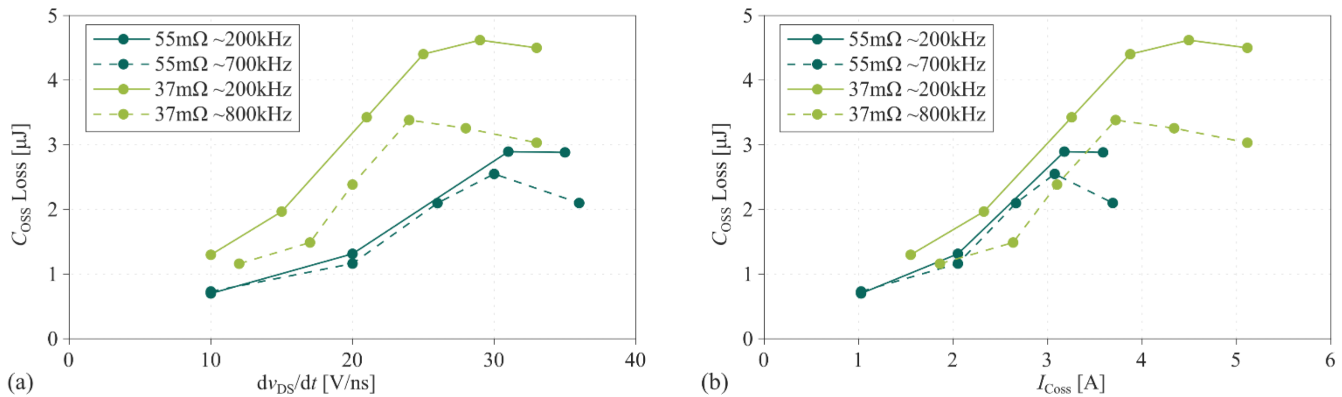

Fig. 6. $R_{DS(ON)}$ comparison: 55 mΩ versus 37 mΩ. These graphs compare the impact of the HEMT on-state resistance, $R_{DS(ON)}$, on C_{OSS} losses. The graph on the left shows how larger chip area (smaller $R_{DS(ON)}$) features larger C_{OSS} losses and larger loss dependency on frequency. The right graph shows C_{OSS} loss dependency based on displacement current I_{COSS}. The I_{COSS} values in the second graph (b) can be obtained using the equation $I_{COSS} = Q_{OSS}/t_{10\%-90\%}$.

Note that for operation between 2 A and 3 A, the two HEMTs have approximately the same loss slope with respect to I_{Coss}. This suggests the fact that the two devices are based on the same or very similar technology, because while a larger area HEMT determines a larger displacement current I_{Coss} (due to its larger C_{OSS}), the larger area HEMT should also feature a smaller equivalent C_{OSS} vertical series resistance (ESR), which, on the other hand, determines smaller C_{OSS} losses.

Summary

This article proposes a further, yet novel, development to the calorimetric approach proposed by ETH Zurich for the characterization of the device losses taking place in GaN power HEMTs. Calorimetric characterization allows engineers to experimentally quantify dynamic C_{OSS} losses in high-frequency GaN power devices. The proposed approach simplifies both the required calibration and measurement procedures by accounting for all thermal cross-couplings within the thermal system. It also speeds the overall measurement procedure by eliminating the need to achieve thermal equilibrium of the system before recording the temperatures of the DUTs.

Finally, with this approach C_{OSS} losses have been measured for two commercially available Infineon CoolGaN HEMTs featuring two different on-state resistance values. The obtained experimental results show the dependency of such losses on V_{DS} waveform slew rate (dV_{DS}/dt), C_{OSS} equivalent displacement current (I_{Coss}), switching frequency (f_{sw}), and device on-state resistance ($R_{DS(ON)}$).

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For more on designing with GaN power devices, see How2Power’s Design Guide, locate the “Popular Topics” category and select “Silicon Carbide and Gallium Nitride”.

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