ISSUE: June 2024

How Active EMI Filter ICs Reduce Common-Mode Emissions In Single- And Three-Phase Applications (Part 4): Loop-Gain Analysis

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A compact and efficient design of the electromagnetic interference (EMI) filter is paramount to reaching the full benefits of electrification in highly constrained operating environments such as onboard chargers (OBCs) for electric vehicles. Through miniaturization of toroidal-cored common-mode (CM) chokes, an active EMI filter (AEF) circuit for CM noise attenuation can substantially increase the volumetric (kilowatts per liter), gravimetric (kilowatts per kilogram) and cost (per kilowatt) density metrics of not just the EMI filter but the overall power circuit implementation.

Part 1 of this article series[1] provided an overview of AEF techniques to diminish the reliance on bulky passive filter components. Parts 2 and 3 discussed behavioral models to characterize the impedance of ferrite[2] and nanocrystalline[3] chokes, respectively. Deriving a choke model is an essential step and of significant importance in EMI filter designs, as the choke impedance directly impacts filter attenuation as well as stability performance in active designs.

To this end, this fourth installment of this series examines small-signal stability[4] by deriving loop-gain expressions for a feedback-type, voltage-sense current-inject (FB-VSCI) AEF circuit implemented using an IC.[1,5] To validate the proposed analytical approach, the article concludes with simulations and experimental measurements applied to a three-phase EMI filter suitable for an OBC application.[6]

Active EMI Filters For Grid-Tied Applications

FB-VSCI AEF Circuit

Fig. 1 shows the schematics for a two-stage CLCL passive-only filter and an equivalent active filter design.

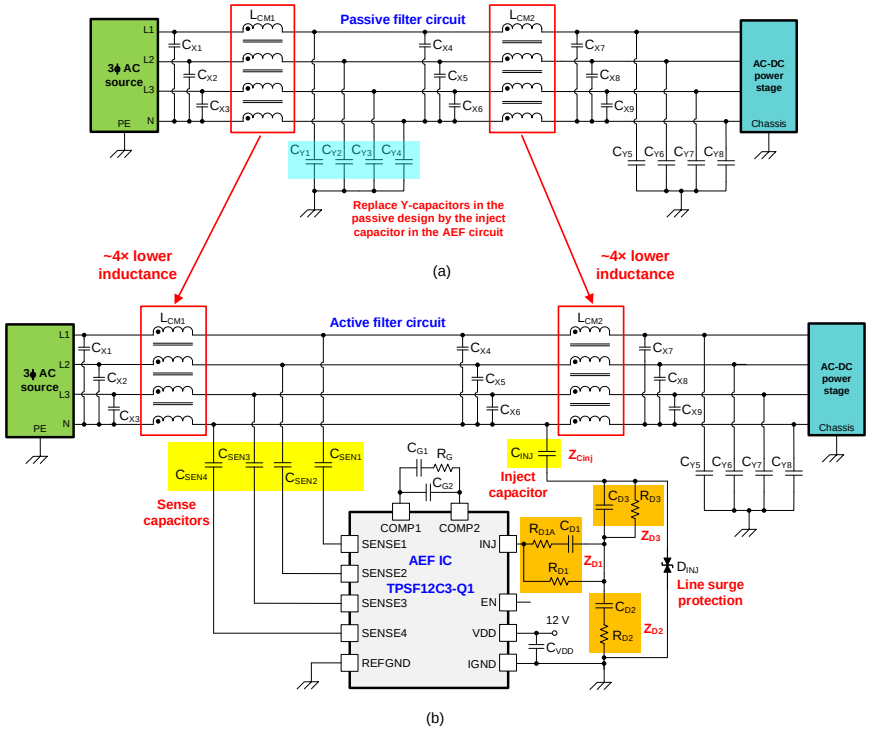

Fig. 1. Schematic of a passive filter (a) replaced by a corresponding AEF circuit (b).

The AEF IC (TI's TPSF12C3-Q1) for this three-phase application is positioned between the CM chokes, designated as L_{CM1} and L_{CM2} in Fig. 1, and provides a lower-impedance shunt path for CM currents to flow to chassis ground.

The goal is to reduce the total filter volume yet maintain low values of the low-frequency earth leakage current using an active circuit that shapes the frequency response of the inject capacitor—effectively multiplying its value at high frequencies. In turn, this amplified inject capacitance over the required frequency range is the key to lower CM choke inductances relative to the values of a passive filter with equivalent attenuation.

The FB-VSCI AEF circuit in Fig. 1b leverages high-voltage Y-rated capacitors, highlighted in light yellow, in combination with low-voltage active circuits for sensing and injection. This method provides a high level of integration and supports high density by eschewing magnetic components for noise sensing and injection. X-capacitors for differential-mode (DM) noise attenuation, designated as C_{X4}, C_{X5} and C_{X6} in Fig. 1 and positioned between the CM chokes, also effectively provide a low-impedance path between the power lines from a CM noise standpoint, up to low-megahertz frequencies (depending on the parasitic inductance of the X-capacitors). This allows current injection directly onto one power line using just one inject capacitor.

Based on clearance spacing rules for routing the power lines, neutral is often routed closest to the IC on the circuit board; thus, Fig. 1b shows it as the designated power line for injection. Up to 25 dB of CM noise attenuation[1] is possible with the AEF circuit in the frequency range from 150 kHz to 3 MHz. Note, however, that this AEF design only tackles CM noise, which mainly affects the choke size; DM noise is not considered here.

Functional Block Diagram

As depicted in the block diagram of Fig. 2, the AEF circuit rejects the line-frequency ac voltage using a two-stage high-pass filter sensing network, while amplifying the detected high-frequency CM noise and maintaining closed-loop stability using an external tunable damping circuit with impedance branches indicated as Z_{D1}, Z_{D2} and Z_{D3} (see also the components with subscript "D" reference designators in Fig. 2).

Components R_G, C_{G1} and C_{G2} connected between the COMP1 and COMP2 pins in Fig. 2 form an impedance Z_G, which behaves as a lead-lag network that sets the AEF amplification gain characteristic in tandem with the feedback impedance, denoted as Z_F. The output of the power amplifier (at the INJ pin) injects the required noise-cancelling signal back into the power lines through a damping network and a Y-rated inject capacitor C_{INJ}, typically set at 22 nF in three-phase applications with a touch-current specification[7] of 3.5 mArms.

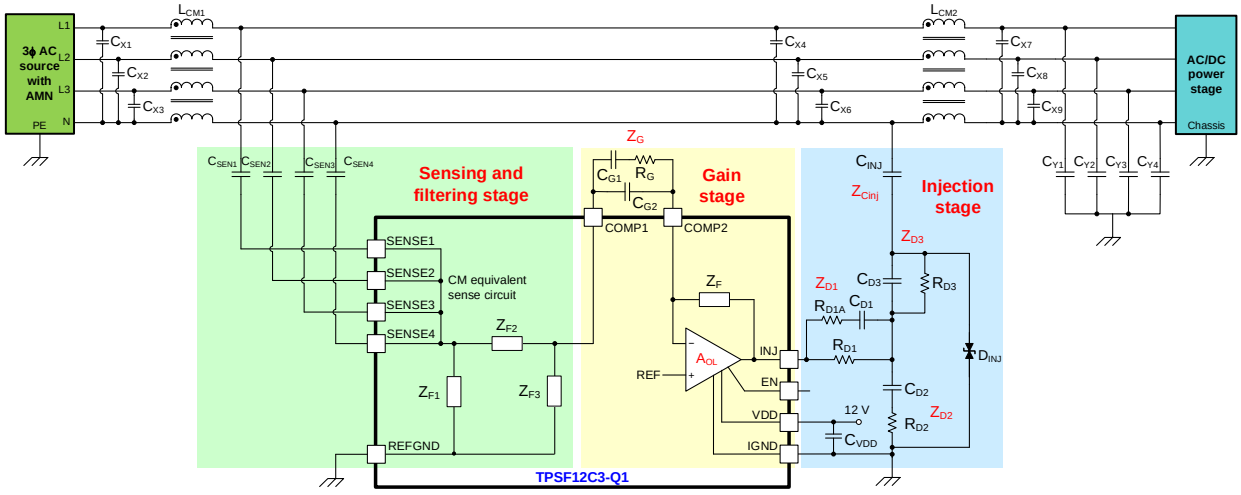

Fig. 2. CM-equivalent functional block diagram of the three-phase FB-VSCI AEF IC.

The purpose of the damping network is to shape the amplifier-output-to-inject-capacitor transfer function and thus stabilize the LC resonant behavior that occurs between the CM choke inductances and the inject capacitance. However, loop stability is an important performance benchmark and must be fully understood and extensively detailed within the scope of a reliable AEF design. Loop-gain expressions are essential to determine small-signal stability margins and extract component values for the requisite compensation and damping networks.

Loop-Gain Derivation

CM Noise Model

Fig. 3 gives a generalized CM circuit model with sensing, gain and inject stages, and the equivalent circuits derived using an amplifier model, as well as grid- and regulator-side Thevenin-equivalent networks. Impedances that appear symmetrically in each phase scale by a factor of "n" for suitable representation in the CM model. More specifically, n = 2 applies to single-phase systems with ground (1p3w); n = 3 pertains to split-phase (1p4w) and three-phase three-wire (3p3w) systems; and n = 4 describes three-phase four-wire (3p4w) systems.

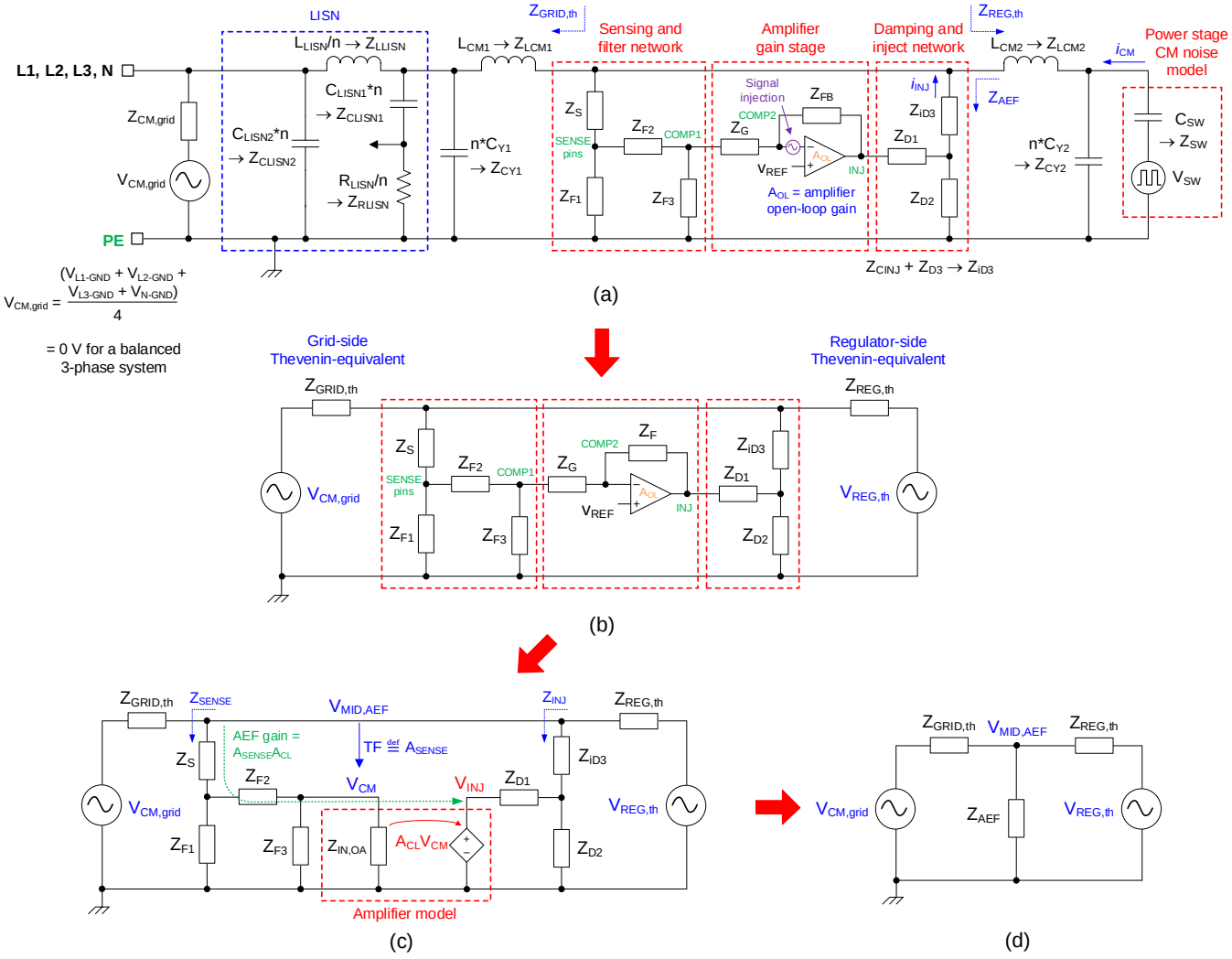

Fig. 3. CM noise model generalized for 1p3w, 3p3w and 3p4w systems with a line impedance stabilization network (LISN) connected at the input (a); circuit reductions (b), (c) and (d).

An equivalent voltage source and capacitive noise source impedance, denoted respectively as V_{SW} and C_{SW} in Fig. 3a, model the power-stage CM noise source. Similarly, an equivalent CM voltage source and source impedance, designated as $V_{CM,grid}$ and $Z_{CM,grid}$ in Fig. 3a, represent the CM disturbance from the grid supply, which should ideally be zero in a balanced three-phase system.

Also included is a model for the LISN, often referred to as an artificial mains network (AMN) when connected at the ac input for EMI measurement. The LISN impedance elements in Fig. 3a also scale by the factor n.

The CM noise model includes the required regulator-side Y-capacitance C_{Y2}, and optional grid-side Y-capacitance C_{Y1}, which appears in parallel with the LISN for high-frequency filtering. Z_S in Fig. 3 is the effective CM impedance of the sense capacitor network, which is part of the high-pass filter along with impedances Z_{F1}, Z_{F2} and Z_{F3} within the IC. Furthermore, Z_F and Z_G denote the impedances of the amplifier gain stage, and Z_{D1}, Z_{D2} and Z_{iD3} interface the amplifier output to the filter injection node between the chokes. As they appear in series, Z_{iD3} in Fig. 3 combines damping impedance Z_{D3} and inject capacitor impedance Z_{CINJ}.

Thevenin-Equivalent Impedances

The grid- and regulator-side Thevenin-equivalent impedances, denoted respectively as $Z_{GRID,th}$ and $Z_{REG,th}$ in Fig. 3, incorporate the applicable passive filter components (CM chokes and Y-capacitors), source parasitic elements, and measurement LISN if connected.

More specifically, equation 1 describes $Z_{GRID,th}$, which combines the choke inductance L_{CM1}, the grid-side Y-capacitors (if installed) and the components for the LISN as shown in Fig. 2, including the grid CM source impedance $Z_{CM,grid}$ if applicable. Meanwhile, equation 2 defines $Z_{REG,th}$, which includes the CM noise source impedance, the regulator-side Y-capacitors and the choke inductance L_{CM2}.

$$Z_{GRID,th}(s) = Z_{LCM1}(s) + Z_{CY1}(s) \left\| \left(Z_{RLISN}(s) + Z_{CLISN1}(s) \right) \right\| \left(Z_{LLISN}(s) + Z_{CLISN2}(s) \left\| Z_{CM,grid}(s) \right. \right) \quad (1)$$

$$Z_{REG,th}(s) = Z_{LCM2}(s) + Z_{CY2}(s) \left\| Z_{SW}(s) \right. \quad (2)$$

Equation 3 defines the Thevenin-equivalent load impedance to the AEF circuit as the parallel combination of $Z_{GRID,th}$ and $Z_{REG,th}$ (see Fig. 3d):

$$Z_{LOAD,th}(s) = Z_{GRID,th}(s) \left\| Z_{REG,th}(s) \right. \quad (3)$$

Equation 4 gives the Thevenin regulator-side voltage source shown in Fig. 3b:

$$V_{REG,th}(s) = V_{SW}(s) \frac{Z_{CY2}(s)}{Z_{SW}(s) + Z_{CY2}(s)} \quad (4)$$

Fig. 4 plots typical impedance magnitudes vs. frequency. $Z_{GRID,th}$ is of lower value and thus determines the behavior of $Z_{LOAD,th}$ at low frequency, whereas $Z_{GRID,th}$ and $Z_{REG,th}$ are of similar value at higher frequency (above approximately 20 kHz in this example), mainly because L_{CM1} and L_{CM2} are of the same value.

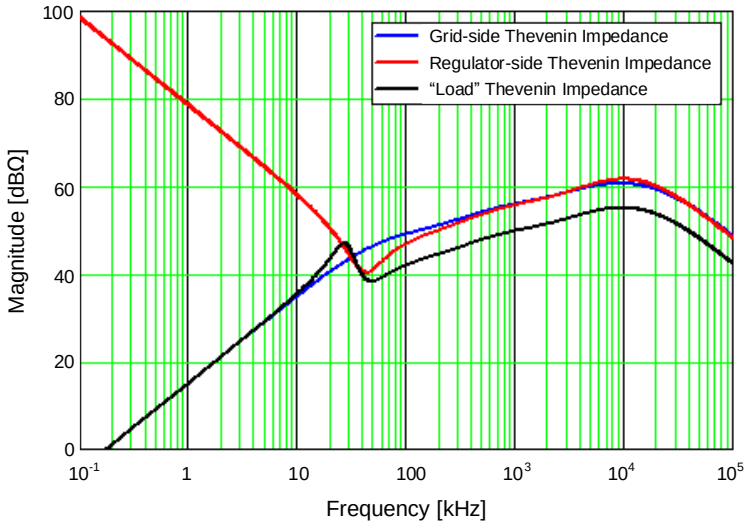

Fig. 4. Typical plots of grid-side, regulator-side and load Thevenin-equivalent impedances, which are denoted as $Z_{GRID,th}$, $Z_{REG,th}$, and $Z_{LOAD,th}$, respectively.

AEF Amplifier Model

Using a conventional model for the amplifier, equation 5 expresses the open-loop gain as

$$A_{OL}(s) = -\frac{A_{DC}}{\left(1+s/\omega_{p,dom}\right)\left(1+s/\omega_{p,par}\right)} \quad (5)$$

where A_{DC} is the dc gain and $\omega_{p,dom}$ and $\omega_{p,par}$ are the dominant and parasitic poles of the amplifier response, respectively.

The amplifier model in Fig. 3c establishes the closed-loop gain, which is effectively the transfer function from the sensed and filtered CM disturbance voltage to the amplifier output at the INJ pin. Equation 6 expresses this closed-loop gain as

$$A_{CL}(s) = -\frac{Z_F(s)}{Z_G(s)} \cdot \frac{1}{1+\frac{\left(1+Z_F(s)/Z_G(s)\right)}{A_{OL}(s)}} \quad (6)$$

The amplifier-stage input impedance shown in Fig. 3c is given simply as

$$Z_{IN,OA}(s) = Z_G(s) + \frac{Z_F(s)}{1+A_{OL}(s)} \quad (7)$$

Leveraging Design-Oriented Analysis

Initiated originally by Prof. David Middlebrook at Caltech and now taught by one of his students, Prof. Dragan Maksimovic at University of Colorado Boulder,[8] we adopt design-oriented analysis (D-OA) techniques here to develop "low entropy" expressions as sequential steps in derivation of the loop gain.

Fig. 5 shows the circuit model for analysis and derivation of the loop gain, with the Thevenin-equivalent load impedance indicated explicitly. You may prefer to skim the following steps of the analysis and proceed to the subsequent sections for a discussion and comparison of the analytical, simulated and experimental results.

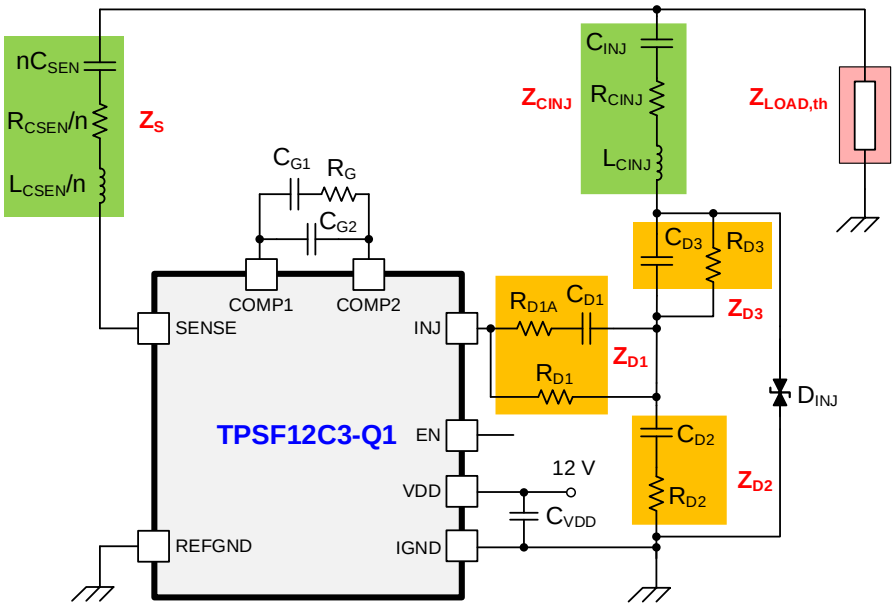

Fig. 5. Circuit model with Thevenin-equivalent load impedance suitable for loop-gain analysis.

The first step in the design-oriented analysis is to derive an expression for the loop gain with no load and no damping (NLND), where impedances $Z_{LOAD,th}$ and Z_{D2} in Fig. 5 are effectively open, and Z_{D1} and Z_{D3} are shorts. Fig. 3a illustrates breaking the loop at the highest impedance point for signal injection; that is, at the amplifier inverting input. Equation 8 expresses this NLND loop gain as

$$T_{NLND}(s) = A_{OL}(s) \cdot \frac{N_1(s) + N_2(s)}{D_1(s) + D_2(s)} \tag{8}$$

where $N_{1,2}(s)$ and $D_{1,2}(s)$ refer to numerator and denominator functions, respectively, as defined by equations 9 through 12:

$$N_1(s) = \left[Z_{F3} \cdot Z_G + Z_{F2} \left(Z_{F3} + Z_G \right) \right] \cdot \left(Z_{CINJ} + Z_S \right) \tag{9}$$

$$N_2(s) = Z_{F1} \cdot \left[Z_{F2} \cdot \left(Z_{F3} + Z_G \right) + Z_G \cdot \left(Z_{CINJ} + Z_S \right) + Z_{F3} \cdot \left(Z_G + Z_F + Z_{CINJ} + Z_S \right) \right] \tag{10}$$

$$D_1(s) = \left[Z_{F3} \cdot \left(Z_G + Z_F \right) + Z_{F2} \cdot \left(Z_{F3} + Z_G + Z_F \right) \right] \cdot \left(Z_{CINJ} + Z_S \right) \tag{11}$$

$$D_2(s) = Z_{F1} \cdot \left[Z_{F2} \cdot \left(Z_{F3} + Z_G + Z_F \right) + \left(Z_G + Z_F \right) \cdot \left(Z_{CINJ} + Z_S \right) + Z_{F3} \cdot \left(Z_G + Z_F + Z_{CINJ} + Z_S \right) \right] \tag{12}$$

Derived using a Mathcad calculator design tool[9] with values from a practical filter design,[10] Fig. 6 plots the loop gain $T_{NLND}(s)$, which comprises a pair of complex-conjugate zeros and two real poles.

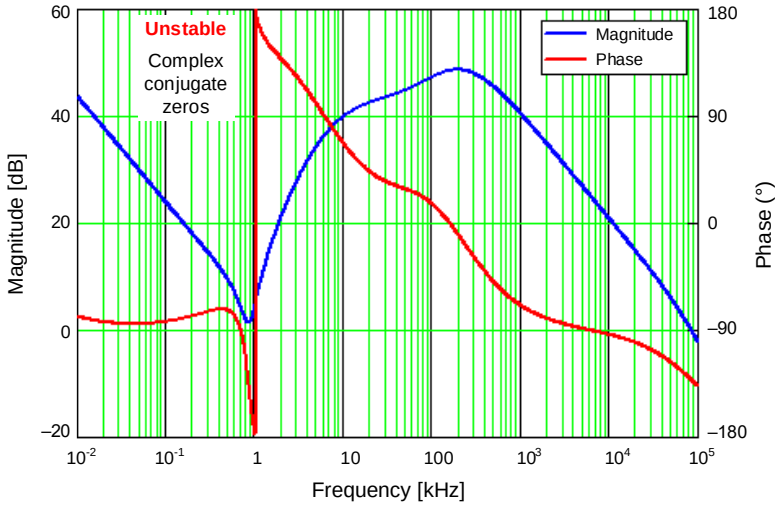

Fig. 6. Loop-gain $T_{NLND}(s)$—no load, no damping.

As a convenient intermediate step, Middlebrook's Extra Element Theorem (EET)[8] helps obtain an expression for the loop gain with load and no damping (WLND). Availing of the open-circuit version of the EET, equation 13 defines the WLND loop gain as

$$T_{WLND}(s) = T_{NLND}(s) \cdot \left[\frac{1 + \frac{Z_{N\_NLND\_to\_WLND}(s)}{Z_{LOAD,th}(s)}}{1 + \frac{Z_{D\_NLND\_to\_WLND}(s)}{Z_{LOAD,th}(s)}} \right] \quad (13)$$

where the quantity in brackets in equation 13 represents the EET correction factor, and $Z_{LOAD,th}$ designates the open-circuit extra element. Equations 14 and 15 derive the nulling and driving-point impedances for the EET as

$$Z_{N\_NLND\_to\_WLND}(s) = Z_{N1}(s) \| Z_{N2}(s) \| Z_{N3}(s) \quad (14)$$

$$Z_{D\_NLND\_to\_WLND}(s) = Z_{CINJ}(s) \| \left(Z_S(s) + Z_{in\_FILT\_D}(s) \right) \quad (15)$$

where $Z_{N1}(s)$, $Z_{N2}(s)$ and $Z_{N3}(s)$ are given by equations 16 through 18, along with terms defined by equations 19 through 21 to simplify the expressions:

$$Z_{N1}(s) = Z_{CINJ}(s) \quad (16)$$

$$Z_{N2}(s) = Z_S(s) + Z_{in\_FILT\_N}(s) \quad (17)$$

$$Z_{N3}(s) = Ratio\_Z_1(s) \cdot Z_{N2}(s) \cdot \frac{Z_{CINJ}(s)}{Z_F(s)} \quad (18)$$

$$Ratio\_Z_1(s) = \frac{Z_G(s)}{Z_{F1}(s)} + \left(1 + \frac{Z_{F2}(s)}{Z_{F1}(s)} \right) \cdot \left(1 + \frac{Z_G(s)}{Z_{F3}(s)} \right) \quad (19)$$

$$Z_{in\_FILT\_N}(s) = Z_{F1}(s) \left\| \left[Z_{F2}(s) + \left(Z_{F3}(s) \| Z_G(s) \right) \right] \right. \quad (20)$$

$$Z_{in\_FILT\_D}(s) = Z_{F1}(s) \left\| \left[Z_{F2}(s) + \left(Z_{F3}(s) \| \left(Z_G(s) + Z_F(s) \right) \right) \right] \right. \quad (21)$$

Fig. 7 shows a plot of the magnitude and phase of $T_{WLND}(s)$, which includes a pair of right-half-plane (RHP) zeros, causing instability.

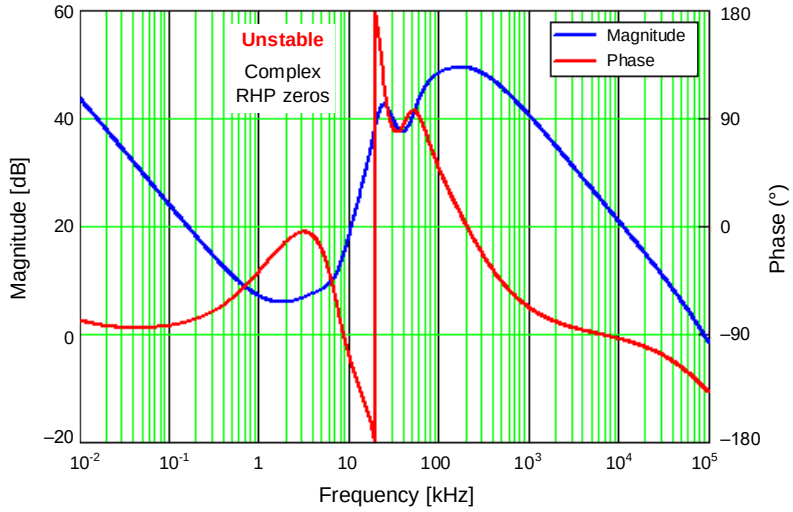

Fig. 7. Loop gain $T_{WLND}(s)$—with load, no damping.

The next step is to perform a star-delta transformation of the damping network elements, going from Z_{D1}, Z_{D2} and Z_{D3} to Z_{dx}, Z_{dy} and Z_{dz}, as shown in Fig. 8.

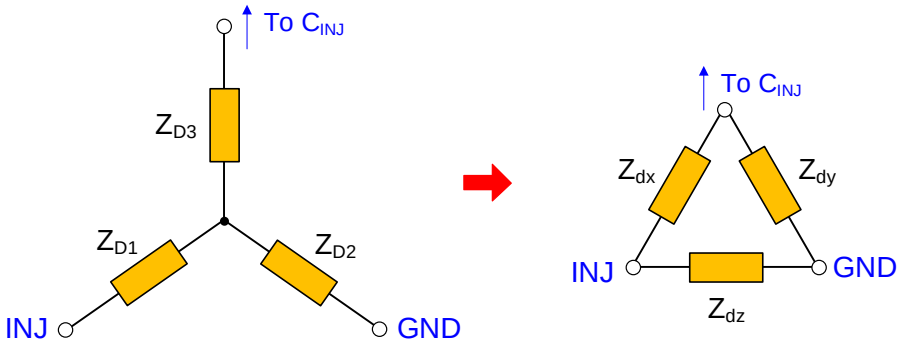

Fig. 8. Star-delta (Y-to-Δ) transformation of the damping network impedances.

Equations 22 through 24 derive the delta-connected impedances in Fig. 8, and facilitate the application of the EET to incorporate the effect of the damping network on the loop gain:

$$Z_{dx}(s) = \frac{Z_{D1}(s) \cdot Z_{D2}(s) + Z_{D2}(s) \cdot Z_{D3}(s) + Z_{D3}(s) \cdot Z_{D1}(s)}{Z_{D2}(s)} \quad (22)$$

$$Z_{dy}(s) = \frac{Z_{D1}(s) \cdot Z_{D2}(s) + Z_{D2}(s) \cdot Z_{D3}(s) + Z_{D3}(s) \cdot Z_{D1}(s)}{Z_{D1}(s)} \quad (23)$$

$$Z_{dz}(s) = \frac{Z_{D1}(s) \cdot Z_{D2}(s) + Z_{D2}(s) \cdot Z_{D3}(s) + Z_{D3}(s) \cdot Z_{D1}(s)}{Z_{D3}(s)} \quad (24)$$

Applying the EET to the WLND gain expression from equation 13 establishes a final WLWD result that combines both the loading effect of $Z_{LOAD,th}$ and the damping effect of Z_{D1}, Z_{D2} and Z_{D3}. Using the short-circuit version of the EET, equation 25 defines the WLWD loop gain as

$$T_{WLWD}(s) = T_{WLND}(s) \cdot \left[\frac{1 + \frac{Z_{dx}(s)}{Z_{N\_WLND\_to\_WLWD}(s)}}{1 + \frac{Z_{dx}(s)}{Z_{D\_WLND\_to\_WLWD}(s)}} \right] \quad (25)$$

where the quantity in brackets designates the EET correction factor with $Z_{dx}(s)$ classified as the short-circuit extra element. Equations 26 and 27 derive the nulling and driving-point impedances, respectively, as

$$Z_{N\_WLND\_to\_WLWD}(s) = \frac{Z_{N\_WLND\_to\_WLWD\_num}(s)}{Z_{N\_WLND\_to\_WLWD\_denom}(s)} \quad (26)$$

$$Z_{D\_WLND\_to\_WLWD}(s) = Z_{BC}(s) \| Z_{dy}(s) \quad (27)$$

The numerator and denominator terms in equation 26 originate as equations 28 and 29:

$$Z_{N\_WLND\_to\_WLWD\_denom}(s) = \frac{Ratio\_Z_2(s)}{Z_{dy}(s)} + \frac{Ratio\_Z_1(s)}{Z_{dy}(s)} \cdot \frac{Z_S(s)}{Z_F(s)} + Y_N(s) \cdot \left(1 + \frac{Z_{CINJ}(s)}{Z_{dy}(s)} \right) \quad (28)$$

$$Z_{N\_WLND\_to\_WLWD\_num}(s) = 1 + Ratio\_Z_2(s) + Ratio\_Z_1(s) \cdot \frac{Z_S(s)}{Z_F(s)} + Y_N(s) \cdot Z_{CINJ}(s) \quad (29)$$

Equations 30 through 33 serve to streamline the previous expressions for loop gain:

$$Y_N(s) = \frac{Ratio\_Z_1(s)}{Z_F(s)} + \frac{Ratio\_Z_3(s)}{Z_{LOAD,th}(s)} \quad (30)$$

$$Ratio\_Z_2(s) = \frac{Z_G(s)}{Z_F(s)} + \frac{Z_{F2}(s)}{Z_{F1}(s)} \cdot \left(1 + \frac{Z_G(s)}{Z_{F3}(s)} \right) \quad (31)$$

$$Ratio\_Z_3(s) = Ratio\_Z_1(s) \cdot \frac{Z_S(s)}{Z_F(s)} + Ratio\_Z_2(s) \quad (32)$$

$$Z_{BC}(s) = Z_{CINJ}(s) + Z_{LOAD,th}(s) \| \left(Z_S(s) + Z_{in\_FILT\_D}(s) \right) \quad (33)$$

Analytical Results

Based on the derived expressions above, Fig. 9 shows magnitude and phase plots for the loop gain $T_{WLWD}(s)$.

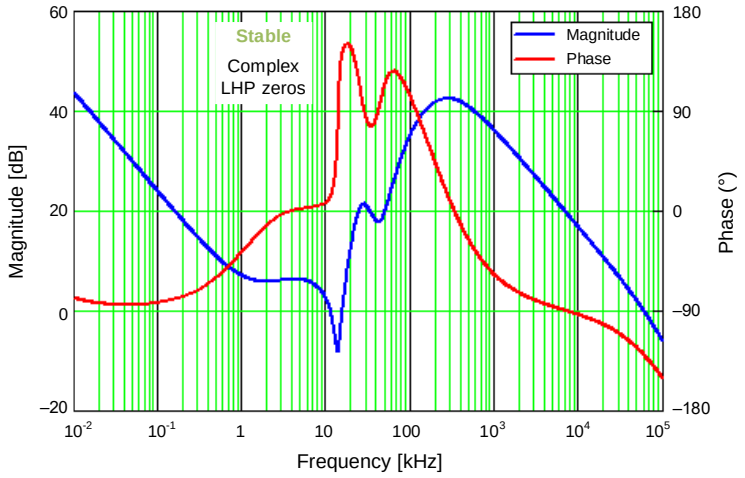

Fig. 9. Loop gain $T_{WLWD}(s)$—with load, with damping.

The damping network converts the complex RHP zeros to left-half-plane (LHP) zeros, stabilizing the system by preventing a negative gain margin from a phase drop to –180° or lower. To avoid a negative gain margin and thus instability, the phase characteristic should be well damped and not reach –180° at the resonant frequencies that typically occur within a range of approximately 2 kHz to 40 kHz.

Simulation And Experimental Results

Simulation Results

Fig. 10 shows a SIMPLIS simulation result using the same three-phase filter design[10] as that used for the analytical results above. The simulated plot demonstrates very close agreement with the calculated plot of Fig. 9, thus confirming the accuracy of the analytical approach.

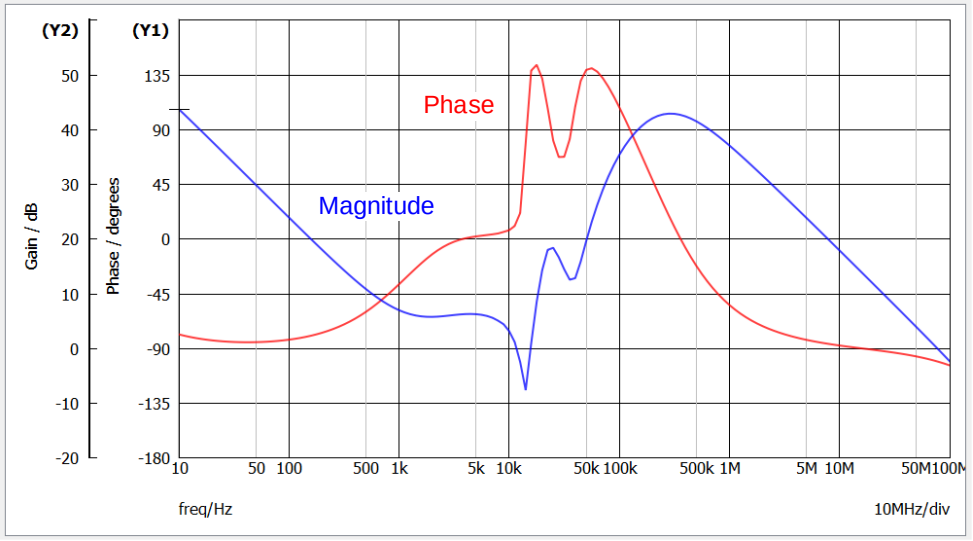

Fig. 10. Simulated loop gain (magnitude and phase).

Practical Results

Fig. 11 shows a 3p4w evaluation module (EVM)[10] rated at 32 Arms per phase specifically for a 22-kW OBC application. The nanocrystalline CM chokes, manufactured by Würth Elektronik, each have a CM inductance of 0.75 mH at 10 kHz, and the Y-capacitors at the grid and regulator sides are 2.2 nF and 6.8 nF, respectively.

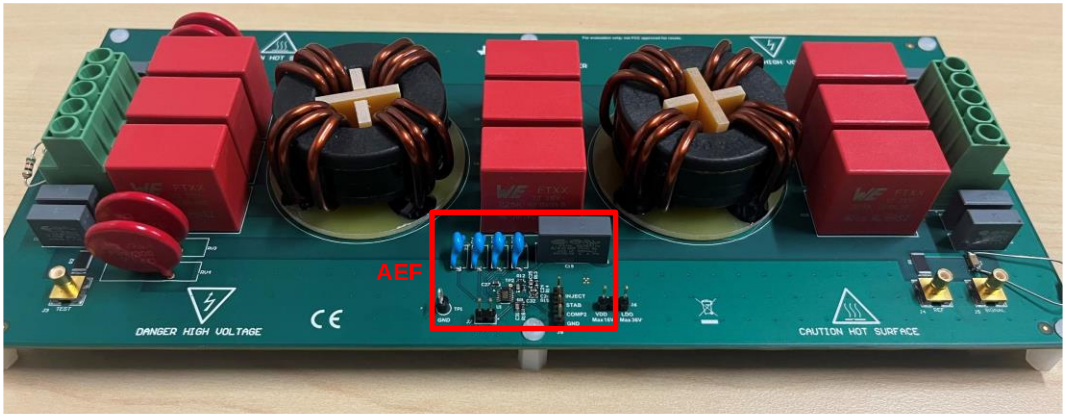

Fig. 11. EVM of a three-phase EMI filter with AEF intended for a 22-kW OBC.

As shown in Fig. 12, I connected a Bode 100 vector network analyzer (VNA) from Omicron Labs, which also functions as a frequency response analyzer, to perform a practical measurement of the loop gain by injecting an isolated excitation signal at the inverting input of the AEF amplifier (see Fig. 3a for the schematic connection of this signal source). The sweep is from 10 Hz to 50 MHz.

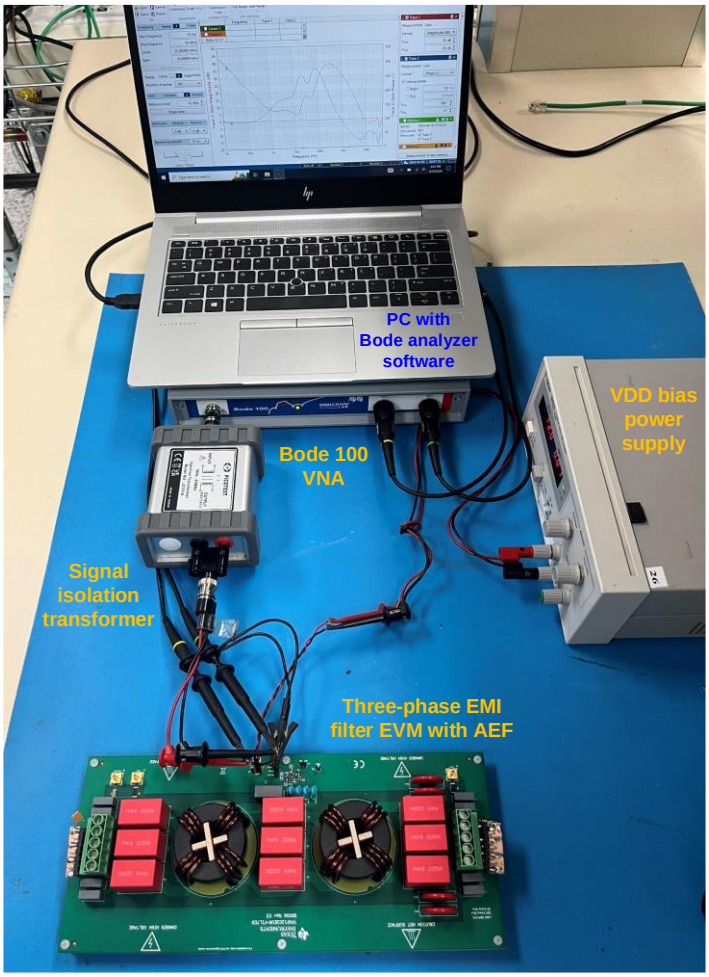

Fig. 12. Loop-gain measurement setup with a Bode 100 VNA and signal injection transformer.

The TPSF12C3-Q1 AEF IC has been specially modified for this test by using focused ion beam (FIB) technology to remove the internally integrated feedback impedance Z_F such that it is possible to apply the excitation signal directly at the amplifier inverting input as needed. The components for impedance Z_F connect externally on the board close to the IC (between the COMP2 and INJ pins, as indicated in Fig. 2).

Fig. 13 shows that the measured loop gain largely aligns with the analytical and simulated results from Fig. 9 and Fig. 10, respectively.

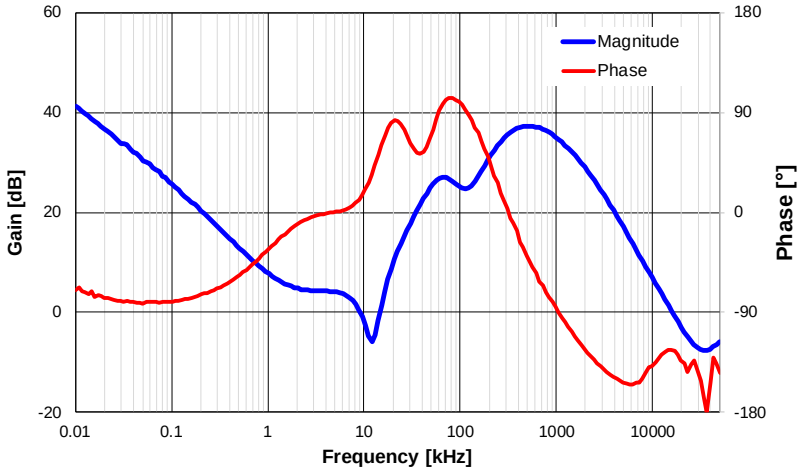

Fig. 13. Experimental loop gain result.

Noteworthy, however, is that the loop crossover frequency in Fig. 13 occurs at 16 MHz, which is diminished relative to the predicted crossover of 60 MHz from Fig. 9. This relates to the capacitive parasitics inherent in the experimental setup. Essentially, breaking the loop and insertion of the excitation signal creates a capacitive loading effect at the high-impedance inverting input of the amplifier, thus causing the loop gain and phase to roll off earlier than predicted.

In addition, the resonant behavior in the 10-kHz to 40-kHz range from Fig. 13 appears more damped than expected. This can be attributed to imprecisions in the resistive part of the modeled choke impedance,[3] which relates to the frequency-dependent permeability of the nanocrystalline core chokes.

Summary

AEF circuits now receive significant attention for power electronics-constrained applications, owing to the attendant improvements in power density and cost of the EMI filter. An efficient, cost-effective and high-density filter is a key challenge in switching regulator designs and is essential to effectually package the overall solution within demanding chassis-enclosed form factors.

This article's analysis centered on the stability of a CM AEF circuit with a supplementary tunable damping network for applicability to single-, split- and three-phase ac-dc applications. Careful manipulation of the basic loop-gain expression by applying the EET—first to include the effect of AEF circuit loading, and second to incorporate a damping network—provided a rigorous derivation of the damped, loaded loop gain for stability analysis. Close agreement of the formulated analytical results, with simulation modeling and experimental loop measurements using a VNA, substantiated the theoretical approach described.

References

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About The Author

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For more on EMI and electromagnetic compatibility topics in power-supply design, see How2Power's Power Supply EMI Anthology.