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Resonant Gate Drive Enhances Robustness Of GaN Power Stages

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Resonance driving of silicon-based power devices has been extensively researched.[1] The use of resonance to save power has been a main focus of this research. In this article, we will show an additional use of resonance—to enhance robustness of circuit operation in GaN power stages. We'll also demonstrate how the uP1964 GaN driver is well suited to such applications.

The uP1964 is a single-channel GaN driver with performance aspects that help solve common issues with high-voltage and low-voltage GaN devices. The uP1964 can be used with lossy ferrite beads in a resonant-gate-drive topology to minimize problems with gate oscillations, improve cross-conduction immunity in half-bridge topologies, and make drive circuit PCB layouts less critical.

This article will discuss these attributes of the uP1964 and demonstrate through simulation and hardware testing the ease of design that this driver allows. Additionally, there will be a focus on the methods required to measure the performance of uP1964-based GaN power stages correctly.

Overview Of The GaN FET Driver

Fig. 1 is a block diagram of the uP1964. The WDFN3x3-10L package pin-out is shown; an alternate 12-pin WLCSP package is also available.

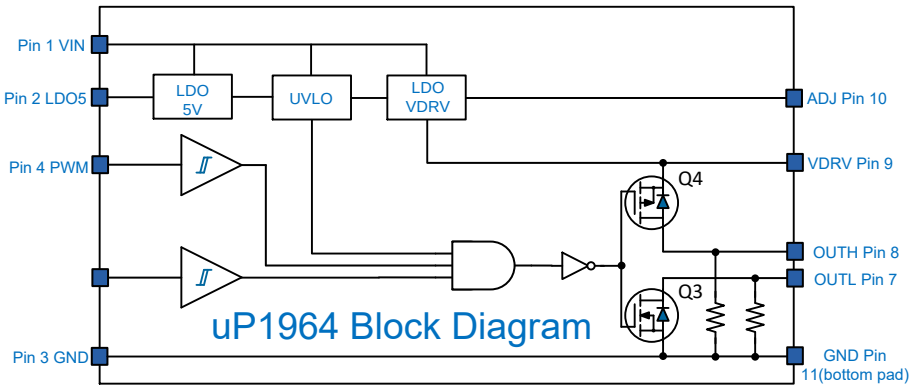

Fig. 1. uP1964 architecture.

The critical aspects of this architecture are

- the ability to adjust the drive voltage to match the GaN technology in use
- the ability of the output(s) to go below ground and above drive-voltage levels
- the allowance of more significant margin in cross-conduction prevention during "Miller" effect
- unregulated input voltages of up to 13 V, allowing simple isolation circuits
- the creation of a regulated 5-V output for powering ancillary circuits.

Basic Operation

Referencing the simulation circuit in Fig. 2, S1 represents the (almost) perfect driver switching between a 5-V source and ground having a 0.5-Ω Z. R1 is the resistor in series with the GaN gate, L2 represents parasitic inductance in the layout, R7 is the gate resistance of the GaN device and C1 represents the gate capacitance.

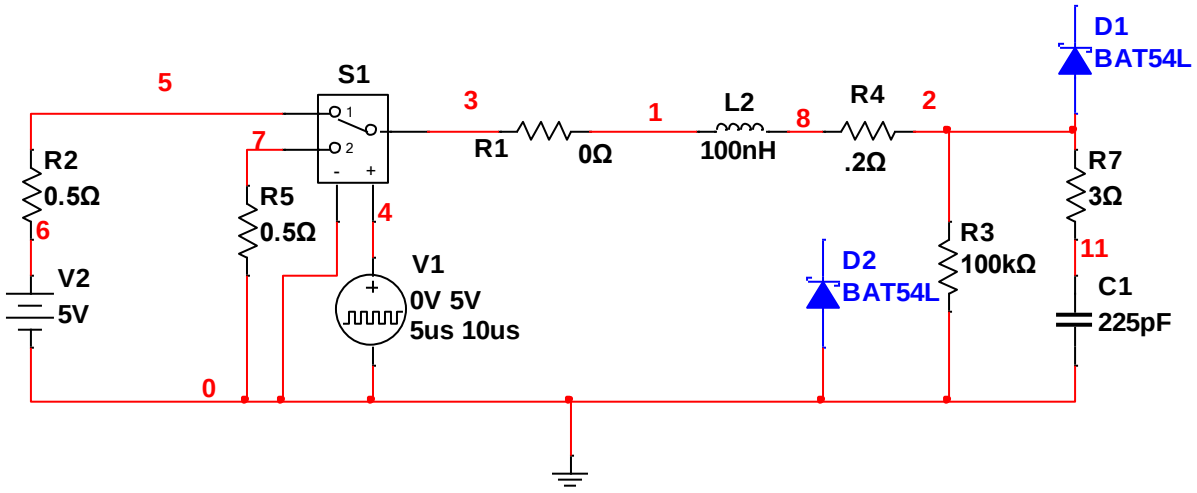

Fig. 2. GaN driver simulation schematic. This circuit represents a "perfect" driver with typical PCB layout inductance.

Looking at the simulation results in Fig. 3 on the rising edge of the voltage on node 3 and node 2, one can observe that there is a large ring due to the resonance of L2, the parasitic inductance of the PCB layout and the gate capacitance C1. The effect of this ringing would be highly stressful on the GaN device, as it has a maximum gate voltage of 7 V. So, this scenario represents a poor PCB layout.

In a real application, the ringing will increase substantially due to the dynamics of the GaN device we are driving. An example will be shown later in this article.

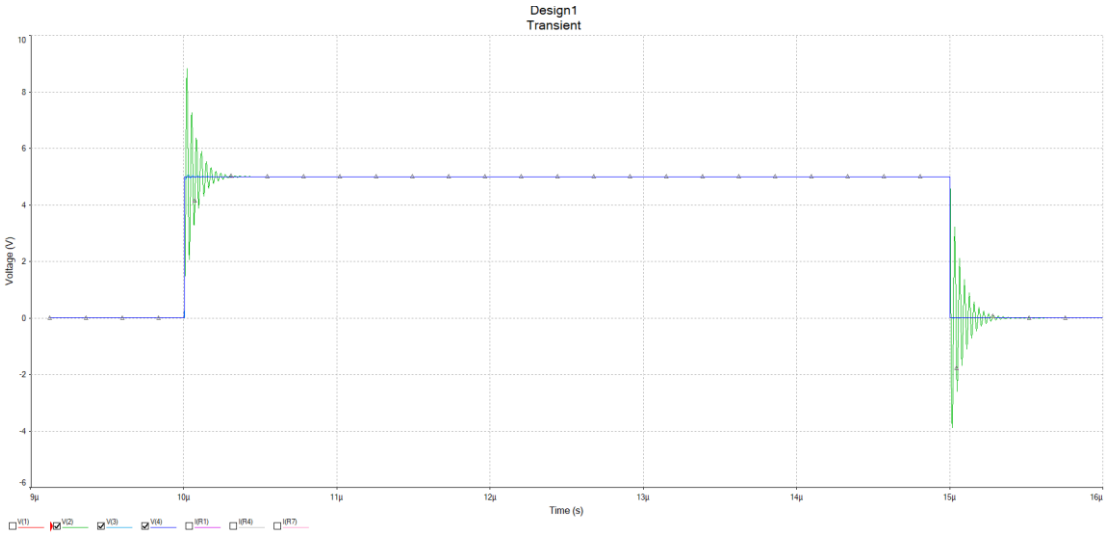

Fig. 3. A simulation of the perfect driver with typical PCB layout inductance. Ringing on nodes 2 and 3 is shown here for the case where R1 = 0 Ω.

In order to overcome the ringing, we can damp the resonance caused by L2 and C1 by increasing the resistance of R1 to a higher value, 22 Ω, shown in Fig. 4. In the simulation result in Fig. 5, we have eliminated the ringing but introduced another problem; slower rise time on the GaN gate (C1 charges more slowly) resulting in increased switching losses.

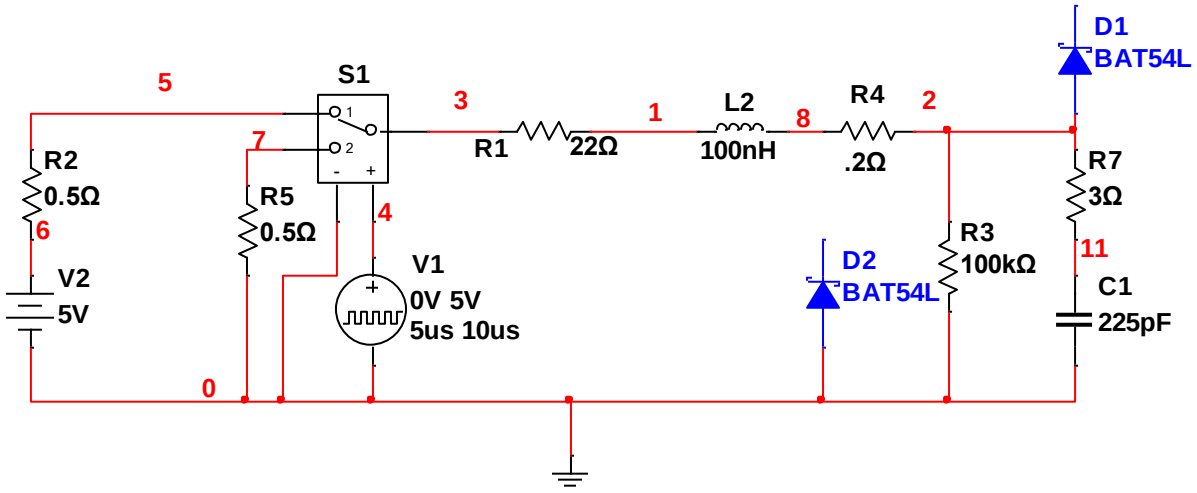

Fig. 4. Perfect driver with typical PCB layout inductance and large damping resistance (R1 = 22 Ω).

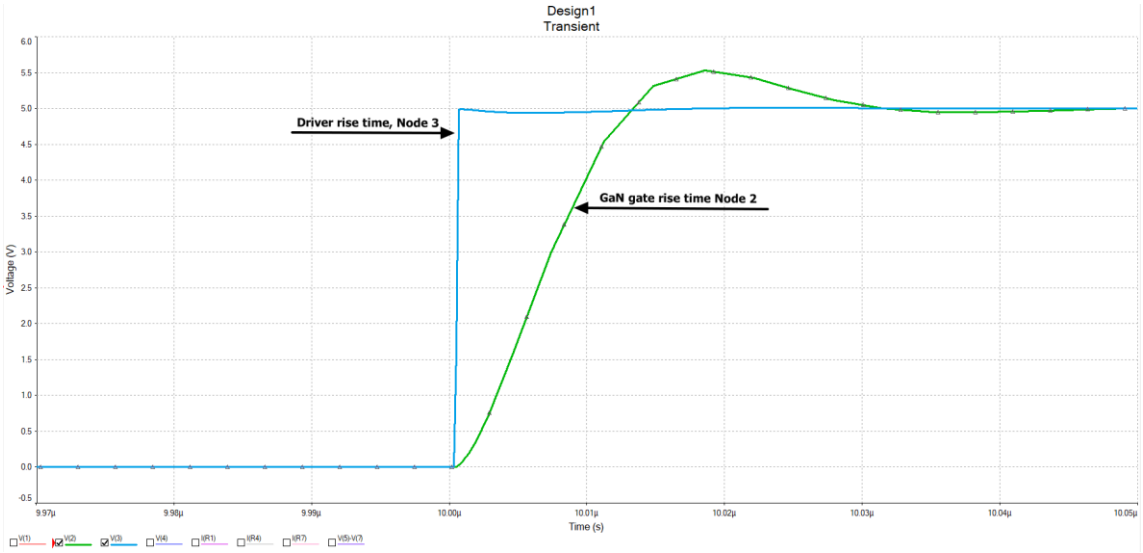

Fig. 5. Simulation of perfect driver with typical PCB layout inductance and large damping resistance (R1 = 22 Ω).

In order to eliminate the issue of a parasitic L2 in the layout, the value of L2 has to be either brought to zero or be swamped out so as not to be relevant to circuit operation. To this end, adding an actual inductor of a known value would not only swamp out the parasitic layout inductance but would also allow variations in layout with less effect on circuit operation.

In Fig. 6, the value of L2 in increased to 733 nH (this is the value of L of the bead we will use in our test circuit). Fig. 7 is then a simulation that shows the effects of adding this increased value inductor (the ringing issue returns as well as reduced rise/fall times).

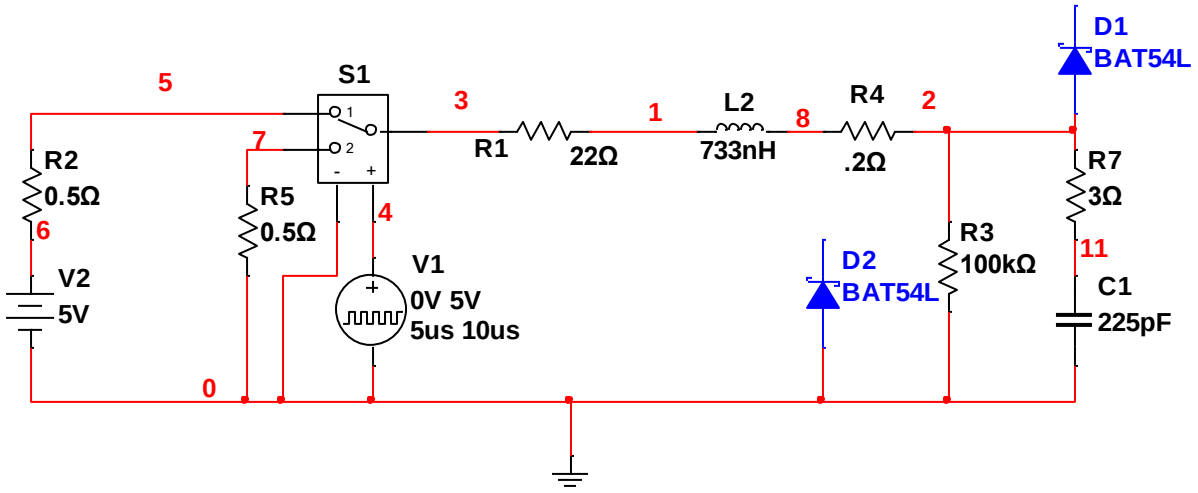

Fig. 6. Perfect driver with increased inductance (L2 = 733 nH) and damping resistance (R1 = 22 Ω).

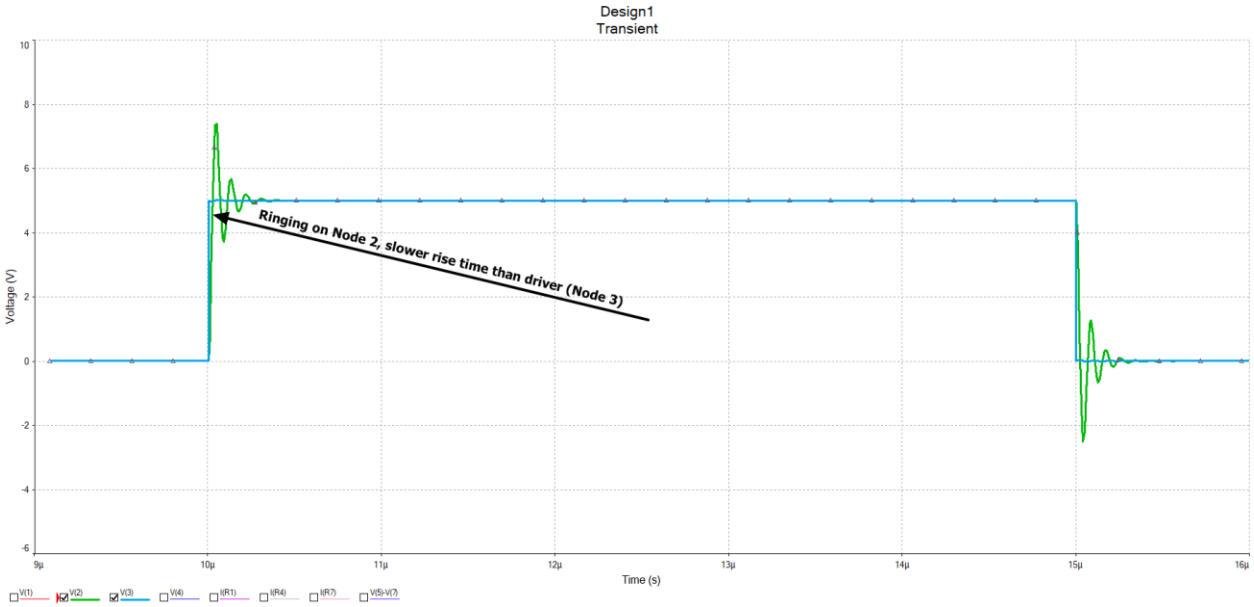

Fig. 7. Simulation of perfect driver with increased inductance (L2 = 733 nH) and damping resistance (R1 = 22 Ω).

With the added inductance, the "ringing" shown in Fig. 7 is still too high and would be destructive to most GaN gates as it reaches an excessive voltage.

In Fig. 8 we add diodes D1 and D2 to the circuit. In Fig. 9, the simulation shows the clamping of the magnitude of the "ringing". Clamping diode, D1, clamps positive excursions, and D2, negative excursions.

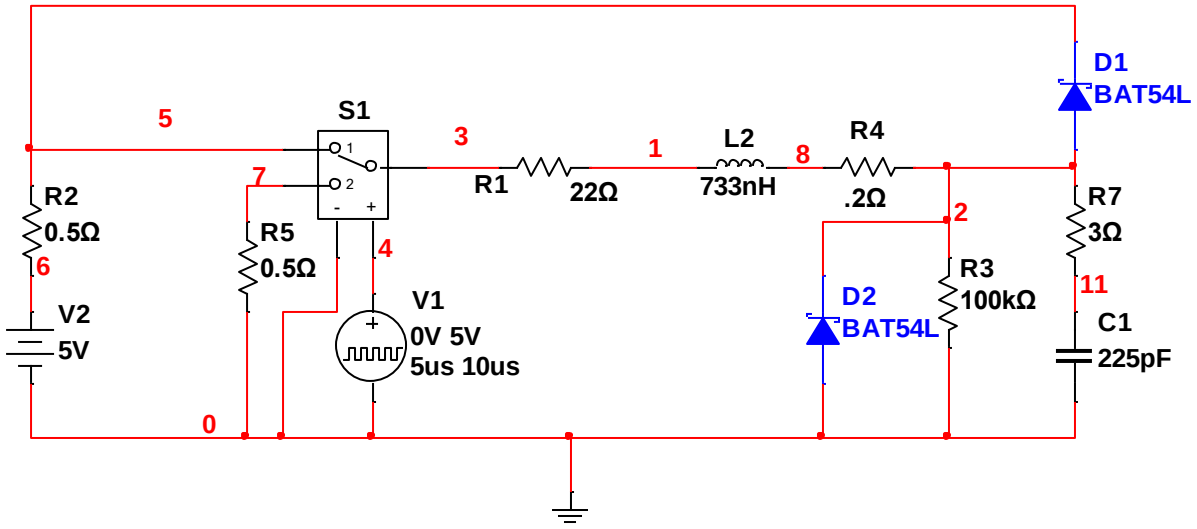

Fig. 8. Perfect driver with increased inductance and damping resistance, and clamping diodes added.

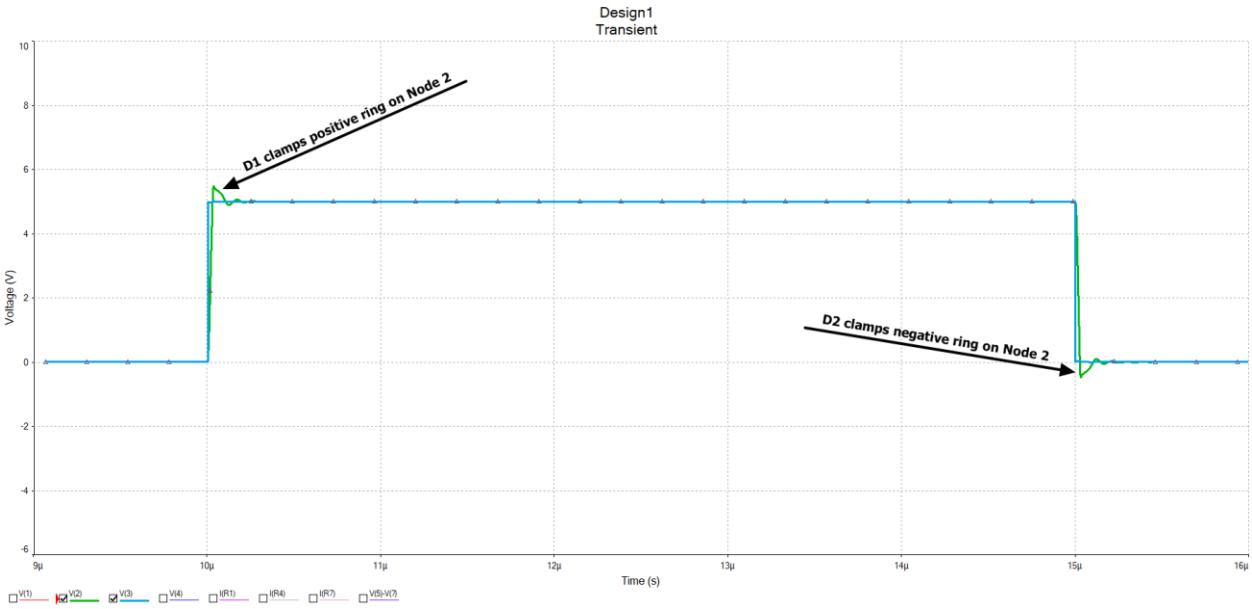

Fig. 9. Simulation of perfect driver with increased inductance and damping resistance plus clamping diodes. Ringing is now within safe limits for the GaN gates.

The simulation in Fig. 9 shows that the ringing is clamped by the diodes, thus the damping resistor, R1, can be decreased in value as displayed in Fig. 10 to improve the rise and fall times.

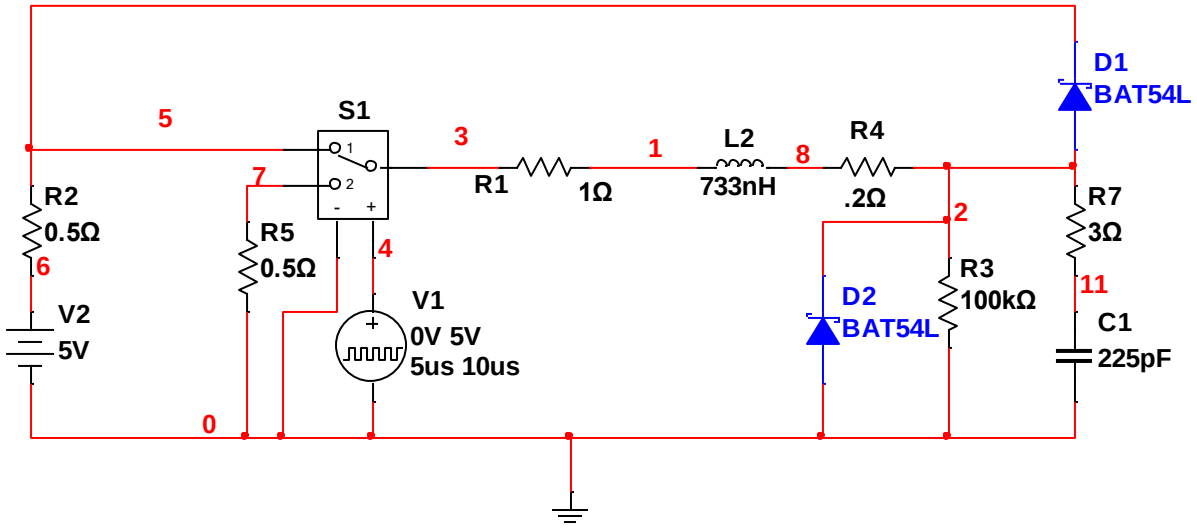

Fig. 10. Perfect driver with increased inductance (L2 = 733 nH), decreased damping resistance (R1 = 1 Ω), and clamping diodes still in place.

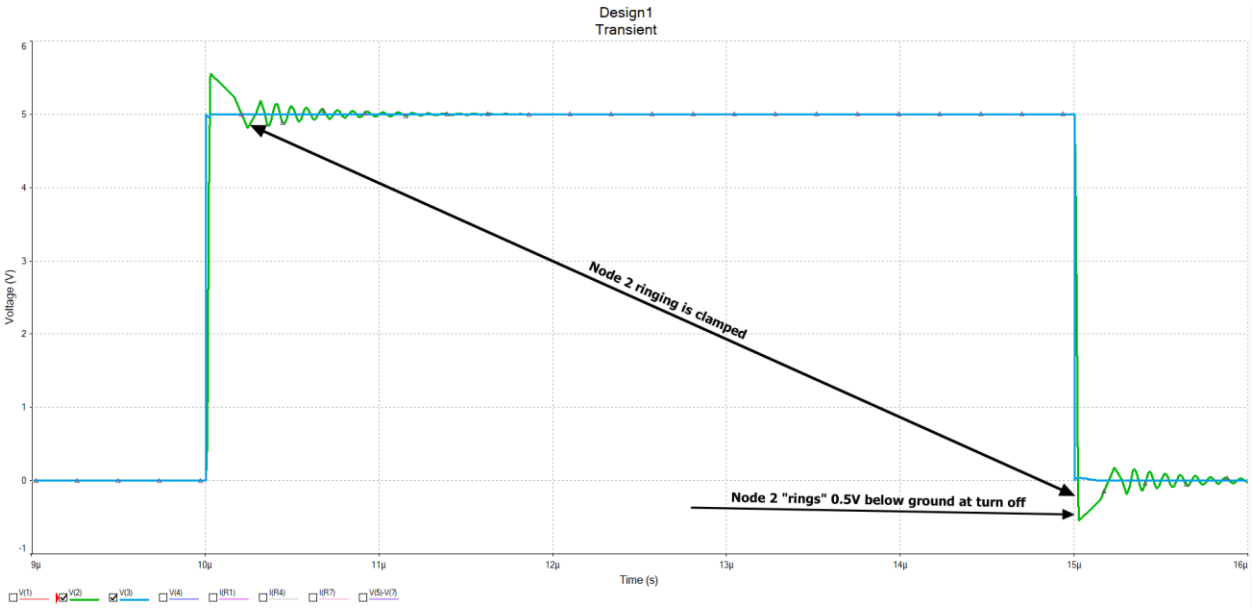

Fig. 11. Simulation of perfect driver with increased inductance (L2 = 733 nH), decreased damping resistance (R1 = 1 Ω), and single clamping diodes still in place.

The simulation in Fig. 11 has the node 2 waveform "ringing" negative to -0.5 V during turn off (going low). This is a key attribute in the application that is supported by the uP1966, as the output pins are specified to go -5 V below ground. GaN devices have gate thresholds that are typically less than 2 V. It is therefore critical that any "spikes" that occur in the gate-drive circuit during switching, such as excursions above ground during Miller capacitance events, be held below this level. The resonant "ring" occurs at the same time as the switching transitions, allowing increased cross-conduction immunity compared to conventional drive circuits.

If one adds another diode in series with D2 and D3 in Fig. 12, the result will be that the negative "ring" will be clamped at a greater negative voltage, -1.0 V, as can be observed in Fig. 13. Note, we have used Schottky diodes as they do not have reverse recovery issues. It might also be possible to use Zener diodes to increase the ring magnitude further negative, but Zener diode response times may be an issue.

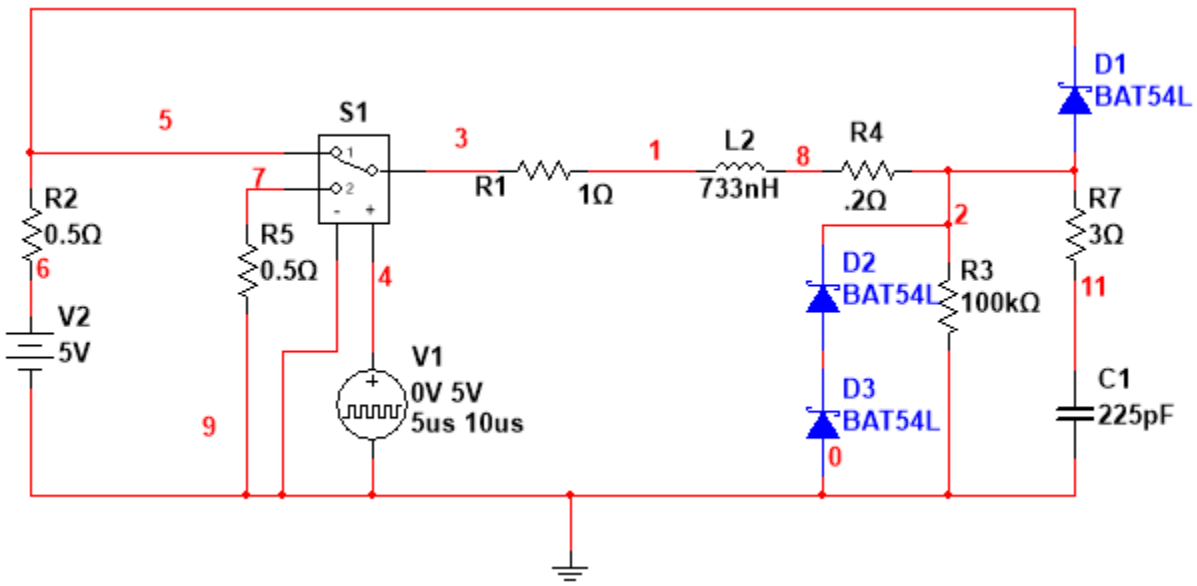

Fig. 12. Perfect driver with increased inductance (L2 = 733 nH), decreased damping resistance (R1 = 1 Ω) and dual clamping diodes (D2 and D3) added.

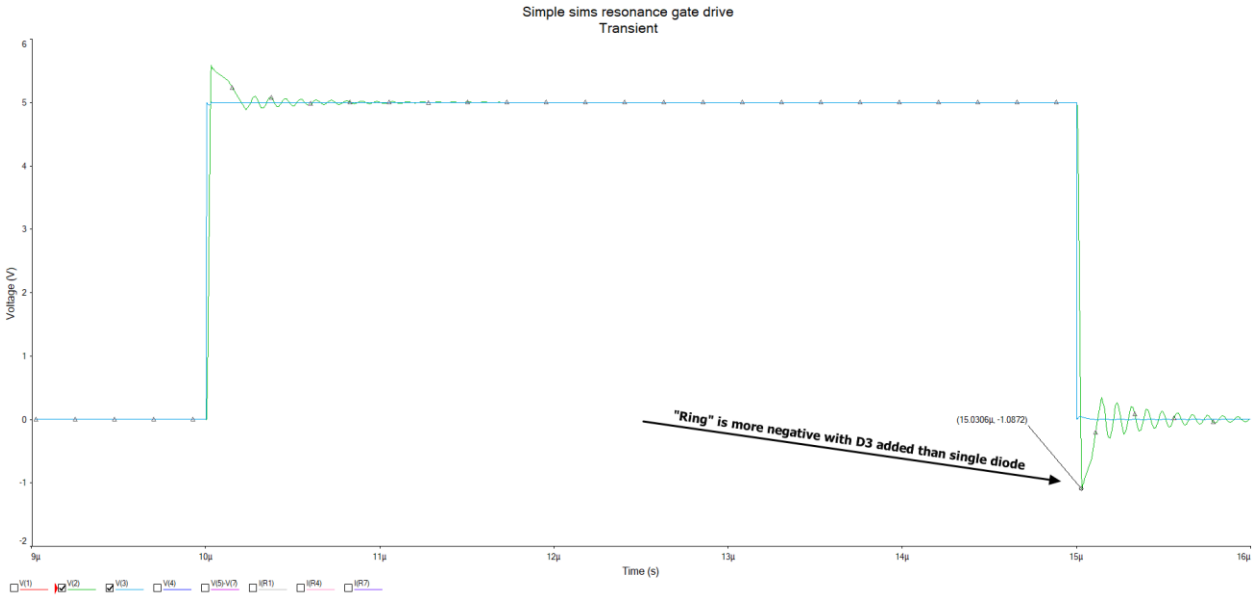

Fig. 13. Simulation of perfect driver with increased (L2 = 733 nH), decreased damping resistance (R1 = 1 Ω) and dual clamping diodes (D2 and D3) added.

These simple simulations convey the concept of circuit operation, but in an actual application there are additional factors such as gate nonlinear capacitance and layout parasitics that are not modeled well. Accurately adding all of these parameters to the simulation would be problematic as PCB stack up, signal routing and GaN device packaging all contribute to the problem.

Validating Circuit Operation Experimentally

To assess that the uP1964 with resonant drive circuitry will work properly in this application, a test platform was built. The test circuit is shown in Fig. 14.

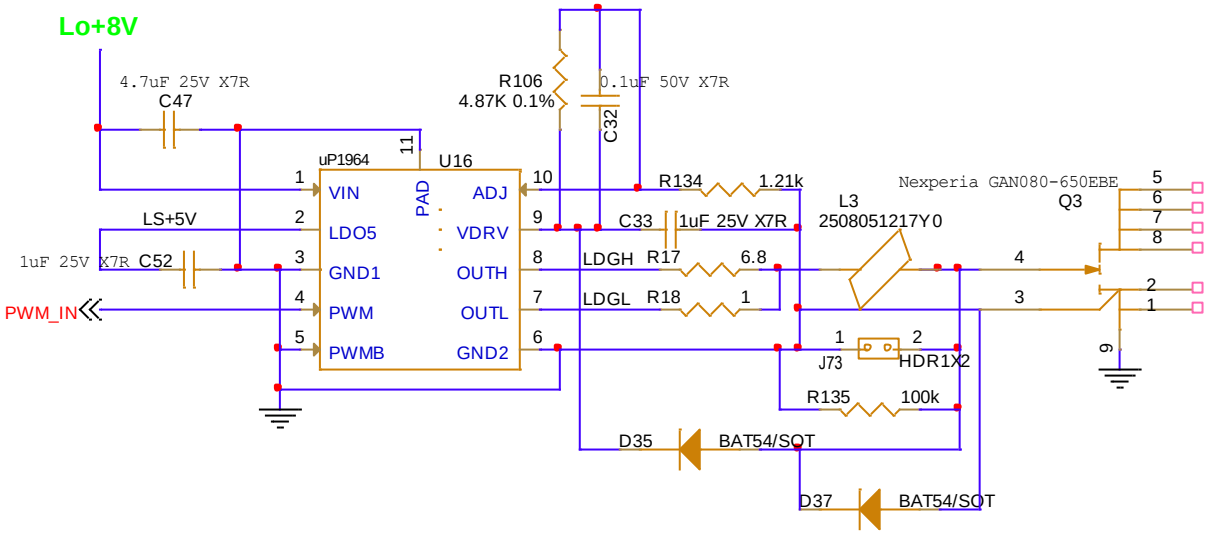

Fig. 14. uP1964 test circuit.

In the uP1964 test circuit, C47 decouples the 8-V to 11-V input power source, while C52 decouples the 5-V LDO internal to the uP1964. R106 and R134 determine the drive voltage for the GaN device, Q3, referenced to an internal 1-V source.

C32 is compensation for the drive-voltage-regulator control loop. C33 is the output capacitor for the drive voltage. R17 sets the current for the resonant gate drive turn-on and R18 sets the current for the turn-off resonance.

R135 is for ESD protection when no circuit bias is present and its value is not critical. The value for R135 can range from 20 kΩ to 100 kΩ. D35 and D37 are the clamping diodes protecting the GaN gate as described previously.

L3 is the "lossy" bead that is used to both cause a "ring" through resonance at both turn-on and turn-off transitions but also—due to its high Z at high frequencies (100-MHz region)—prevents gate oscillations due to parasitics in the layout and switching dynamics in the GaN device.[2]

Test Circuit Platform Description

The schematic below in Fig. 15 represents the platform used to verify the operation and performance of the uP1964 in higher-voltage (400-V) applications.

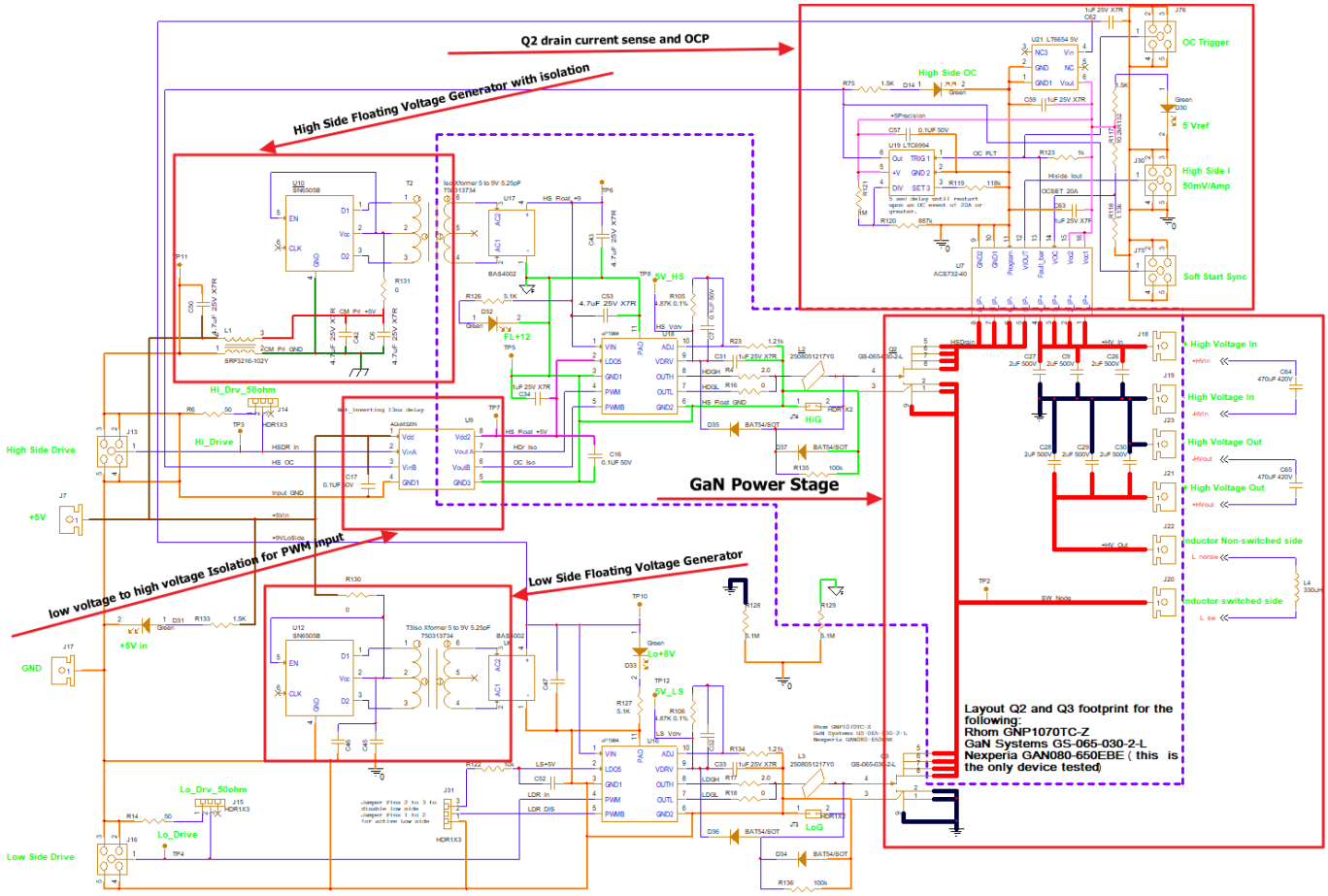

Fig. 15. Schematic of test platform to verify circuit operation in high-voltage applications.

Bias Power Structure

Referring to Fig. 15, the +5-V input on J7 supplies all required drive power for the test platform. The +5 V powers two push-pull drivers, U10 and U12, which are used to transfer power through isolation transformers T2 and T3. These transformers, Würth 750313734, have minimal interwinding capacitance between primary and secondary to reduce any common-mode currents due to the high dv/dt generated by the switching action of the GaN FETs and, through their isolation capacity of 5 kV, can assure "clean" ground paths. An additional measure to prevent common-mode noise is the use of a common-mode choke, L1, in series with the power lines supplying U10.

The output of the isolation transformers are then fed to Schottky bridge rectifiers U17 and U6 for rectification filtered by C43 and C47, creating dc outputs at approximately 9 V. Note that these two 9-V outputs, "HS_Float_+9" and "+9VLoSide" are unregulated and will change with frequency of operation of the power stage, size of the GaN devices being driven and +5-V input voltage variations.

The power rails, "HS_Float_+9" and "+9VLoSide", are then fed to the uP1964 drivers, U18 and U16, where their respective 9-V outputs are regulated by the two LDOs within each uP1964 to provide fixed outputs of 5 V, "HS_Float_+5V" and "LS+5V", and the adjustable drive voltages, "HS_Vdrv" and "LS_Vdrv". The HS_Float_+5V from the uP1964, U18, is also used to power the secondary side of U9, the signal isolator for the high-side input signal, "HSDR_In". Additionally, the "+9VLoSide" is used to power U21 in the "Q2 drain current sense and OCP" section.

Grounds

In Fig. 15 there are four grounds, "Input_GND," "CM_Pri_GND," "HS_Float_GND" and "–Hvin".

"Input_GND" is used as the reference for the signal inputs "HSDR_In" (high-side drive) and "LDR_In" (low-side drive) and all circuits related to U16, the uP1964 driving Q3. As Q3 has a separate Kelvin connection, pin 3, the practicality is that "–Hvin" and "LDR_In" are connected within Q3. R128 is therefore not needed.

"HS_Float_GND" ties to "Input_GND" through R129, a 5.1-MΩ resistor, to prevent "HS_Float_GND" from floating to an unsuitable voltage.

"CM_Pri_GND" does not float (in the dc sense) as it is tied to "Input_GND" through common-mode choke L1.

High-Side (Q2) Drain Current Monitor

U7 is used to both monitor the drain current and to detect an overcurrent event in the top side GaN, Q2 (Fig. 16). It has a limited bandwidth of 1 MHz. U21 acts as a reference for the OCP trip level and as a 5-V regulator to generate the +5Precision net that powers U7 and U19. U19 is a one shot set for 5 seconds that is triggered on an OCP. HS_OC is fed to J75, the Soft Start Sync output, for use if there is a closed-loop control system added to this platform. The OCP has not been tested.

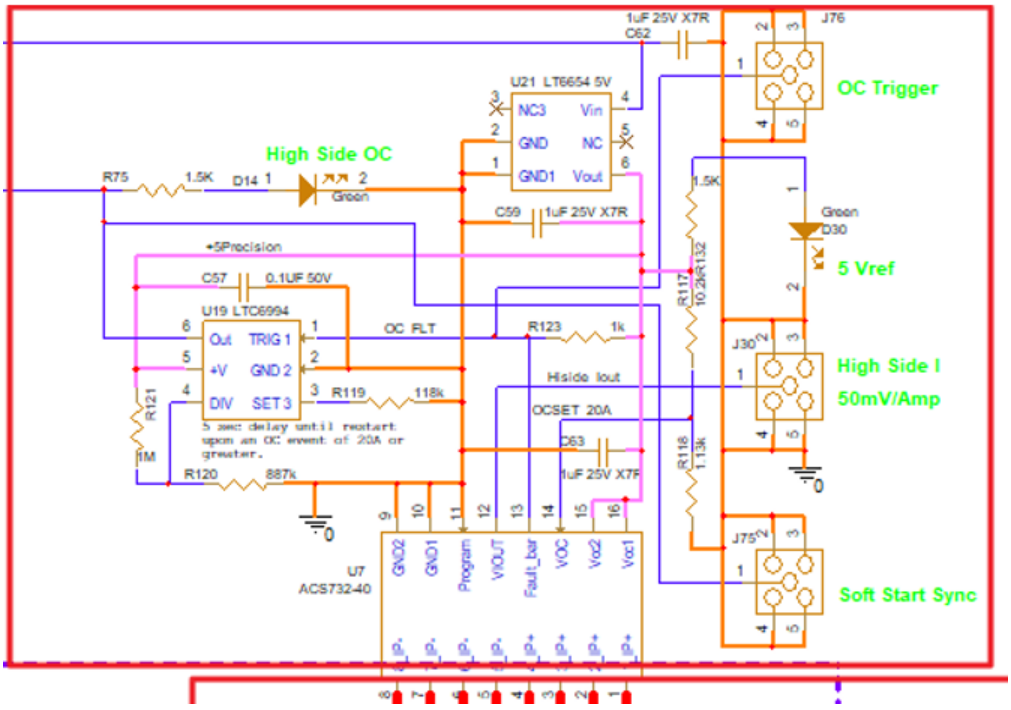

Fig. 16. Close-up of drain current monitoring circuitry from Fig. 15.

GaN Power Stage

The power stage in Fig. 15 (shown in close-up in Fig. 17) is a half bridge, Q2 for the high-side switch and Q3 for the low-side switch, utilizing two Nexperia GAN080-650EBE GaN FETs. These are 80-mΩ 650-V normally off e-mode devices.

For the purpose of our tests, the test platform will be used as a synchronous buck converter. The switched node, SW_Node, is routed to an external inductor through J20. The use of an external inductor allows the test platform to be operated at different test conditions of input voltage, frequency and output load.

Capacitors C27, C26 and C9 are ceramic high-frequency decoupling while bulk input capacitance, C64, is attached through J18 and J19. C28, C29 and C30 are high-frequency ceramic output capacitors with C65 supplying bulk output filtering.

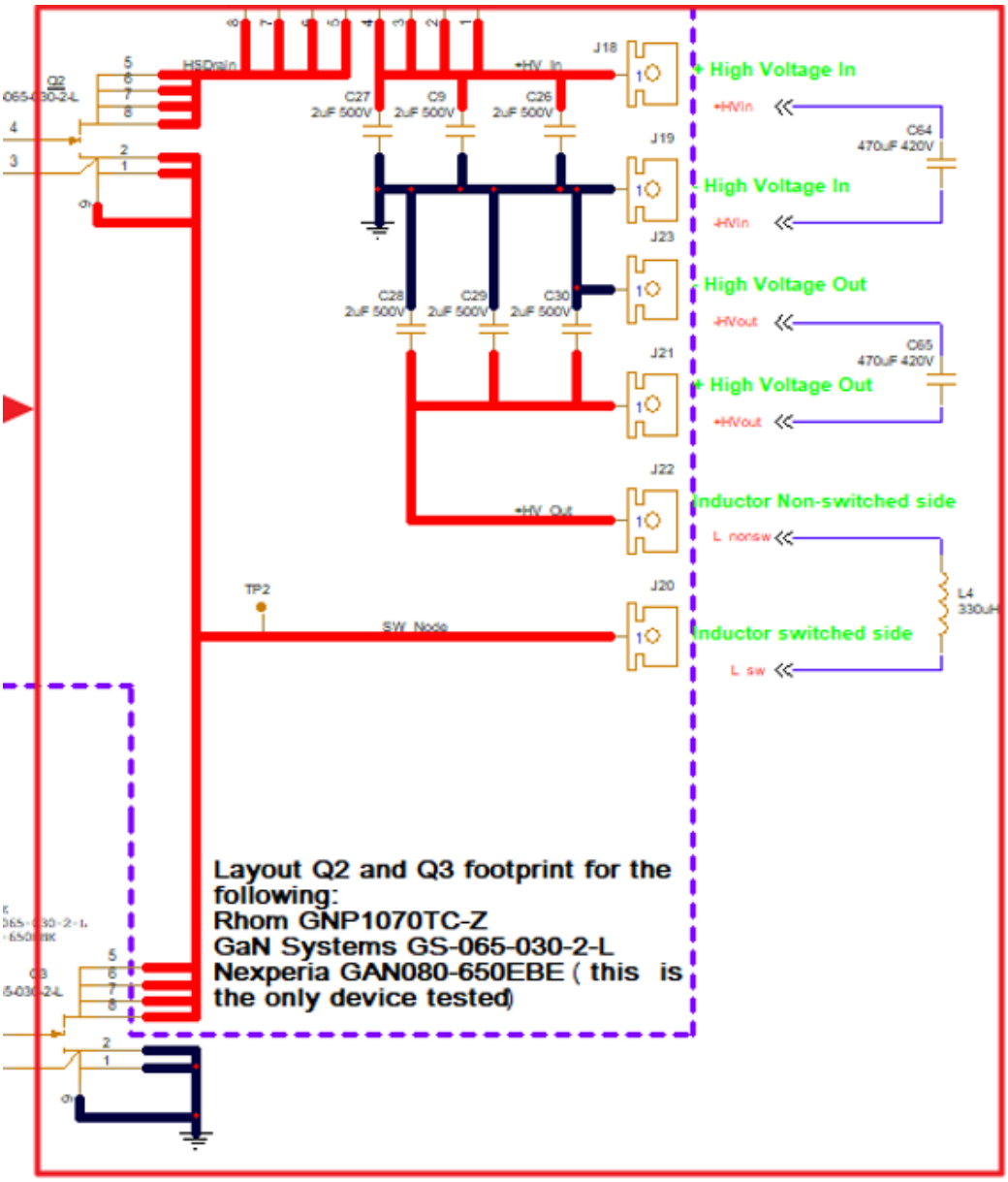

Fig 17. Close-up of GaN power stage components from Fig. 15.

Test Platform Setup

The PCB was designed with the two GaN devices, Q2 and Q3, mounted on the backside of the PCB for conduction cooling. This would be considered to be a less-than-optimal layout from an electrical perspective. The gate-drive signals from the uP1964, which is mounted on the opposite side of the PCB, need to go through vias in the PCB, adding parasitics to the circuit.

Conduction cooling of Q2 and Q3 is through a chiller plate that is kept at a constant 6°C (Fig. 18). The temperatures of the GaN devices are continuously monitored via thermal imaging.

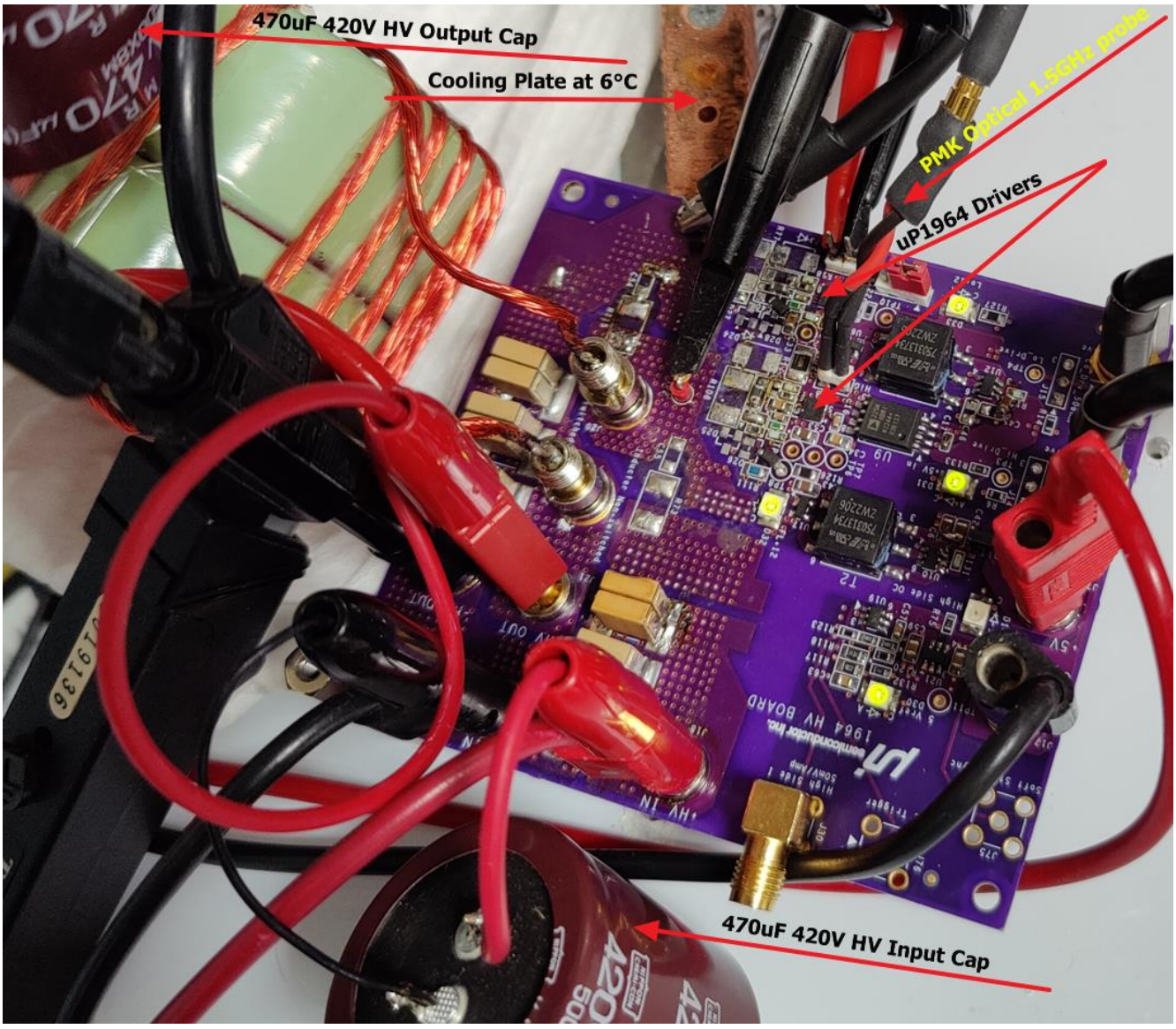

Fig. 18. Test platform setup.

GaN FET Driver Capability

In the test platform, we measured the performance of the uP1964 in circuit to determine operational stresses. The oscillographs below in Figs. 18 and 19 are measured with a PMK FireFly probe with a 10x attenuator on the gate signal for Q3 in Fig. 15 with no input power to +HVin.

Referring to Fig. 18, on the oscillograph, on the left is the waveform at the intersection of R17 and R18 in Fig. 15 while the oscillograph on the right is the waveform at the gate of Q3 in Fig. 15. The result of having a resonant circuit formed from L3 and the gate C of 225 pF of Q3 is that the output of the uP1964 will be subjected to an overshoot of 6.28 V. This is above the Vdrv level of 5 V, but the output of the uP1964 has a 15-V absolute maximum rating. The 1.23-ns rise time is helpful in starting the resonance (ringing the bell).

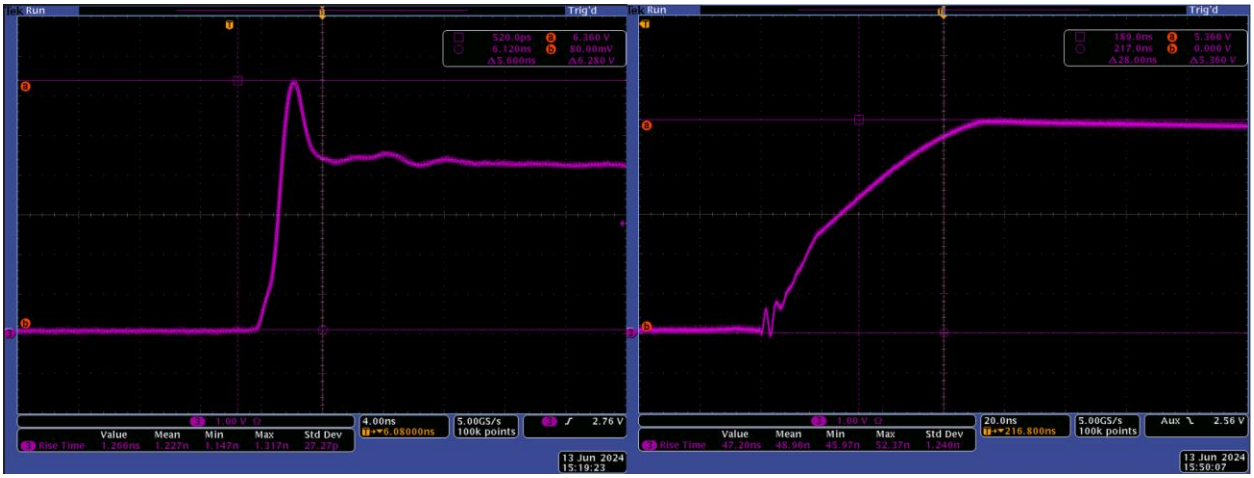

Fig. 18. uP1964 rise time and overshoot stress with Q3 gate drive.

Referring to Fig. 19, on the oscillograph on the left is the waveform at the intersection of R17 and R18 in Fig. 15 while the oscillograph on the right is the waveform at the gate of Q3 in Fig. 15. The result of having a resonant circuit (consisting of L3 and the gate C of 225 pF of Q3) is that the output of the uP1964 will be subjected to a voltage excursion of 1.52 V below ground.

Although this undershoot is below ground, the output of the uP1964 has a -5.0-V absolute maximum rating. Again, as in the rise time example of Fig. 17, the fast 900-ps fall time of the uP1964 is helpful in starting the resonance (ringing the bell).

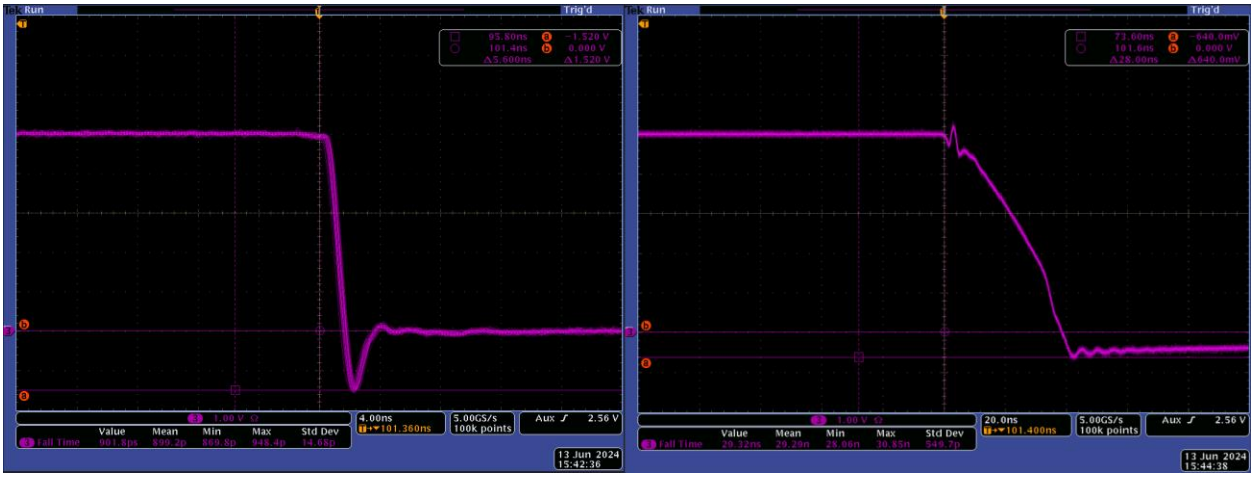

Fig. 19. uP1964 fall time and overshoot stress with Q3 gate drive.

Test Results

As mentioned previously, the layout was deliberately "poor" electrically.

Fig. 20 is an example of this platform's poor electrical performance when used without a resonant drive. In the oscillographs below CH2 blue, is the gate of Q3, measured with a Tektronix TMDP0200; CH3, magenta, is the gate of Q2, measured with a PMK FireFly; and CH4, green, is the switch node, (SW_NODE) at TP3 measured with a Tektronix P6139A 10X passive probe. The HVin was set to 100 V, and the output load was set to 49.7 V at 0.517 A (25.7 W).

The left oscillographs are where the beads, L2 and L3, are replaced with a short; the right oscillographs are with the beads in circuit.

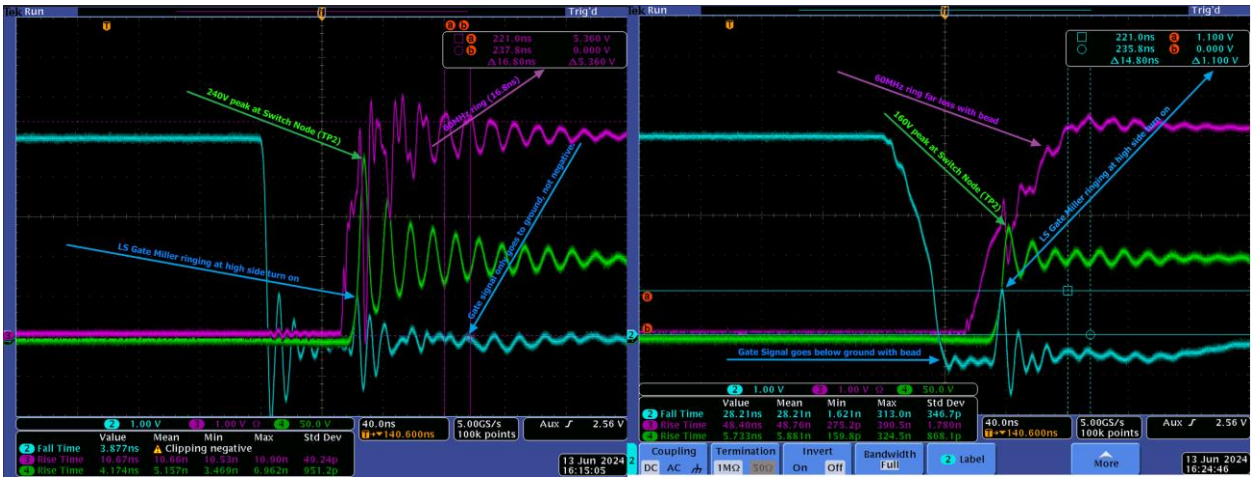

Fig. 20. Test platform electrical performance with and without resonance (beads).

The following observations can be made of Fig. 20:

- The left oscillographs (no bead) display far faster rise and fall times on the gates than the ones to the right. Yet the rise time of the switch node is very similar in both.
- Gate ringing directly affects the high-side drain (GaN is very responsive; fast!) This ringing indicates the frequency region where the bead should be "lossy".
- There appears to be more margin when the Miller spike (Q2 turns on) with the bead in place as the gate is pulled below ground due to the negative "ring". The measurement of the ring on Q3 might not be accurate due to common-mode noise, as the TMDP0200 does not have sufficient common-mode rejection at such high frequencies. We will explore this measurement problem next.

Measurement Issues

Measuring signals such as GaN gate drives which are of a low magnitude relative to the high-voltage switching that results from these signals has historically been very difficult. This is due to the common-mode interference that occurs from the dv/dt that occurs at the switching nodes of the high-voltage power stages. Optically isolated probes, such as the PMK FireFly probe, exhibit high common-mode immunity and as such obtain better fidelity in measuring these signals. One study[3] found that conventional differential probes display as much as a 10-V difference in common-mode interference compared to the optical probes.

Utilizing a Tektronix DPO4104 oscilloscope, we have compared the fidelity of the PMK FireFly optically isolated probe (1.5 GHz) to a Tektronix TMDP0200 differential probe (200 MHz) and a Tektronix P6139A 10X single ended passive probe (500 MHz), on the gate drive to Q3 in Fig. 15. This comparison occurs with the circuit operating with a 400-V input, 280-W output, 78-kHz switching frequency and 30% duty cycle. The result is shown in Fig. 21 where we can see the Miller spike occurring during Q2's turn-on.

One might expect the TMDP0200 to show less of a spike due to its lower bandwidth, but this is not the case. Even though this is a measure of the low-side drive, the common-mode currents still affect the accuracy of the single-ended P6139A passive probe. We can conclude then that all our critical measurements, such as Miller spike magnitude, should be done with an optical probe like the PMK FireFly.

During testing routines if one can affect the shape of the waveform on the oscilloscope simply by touching the cable from the probe then that measurement is being affected by common mode and should be suspect. This

was the case with both the TMDP0200 and the P6139A. Additional information on the effects of common mode on fidelity is provided in reference 4.

Fig. 21. A three-probe comparison of waveform fidelity.

Fig. 22 shows the actual Miller spike at 600-W output, 400-V input.

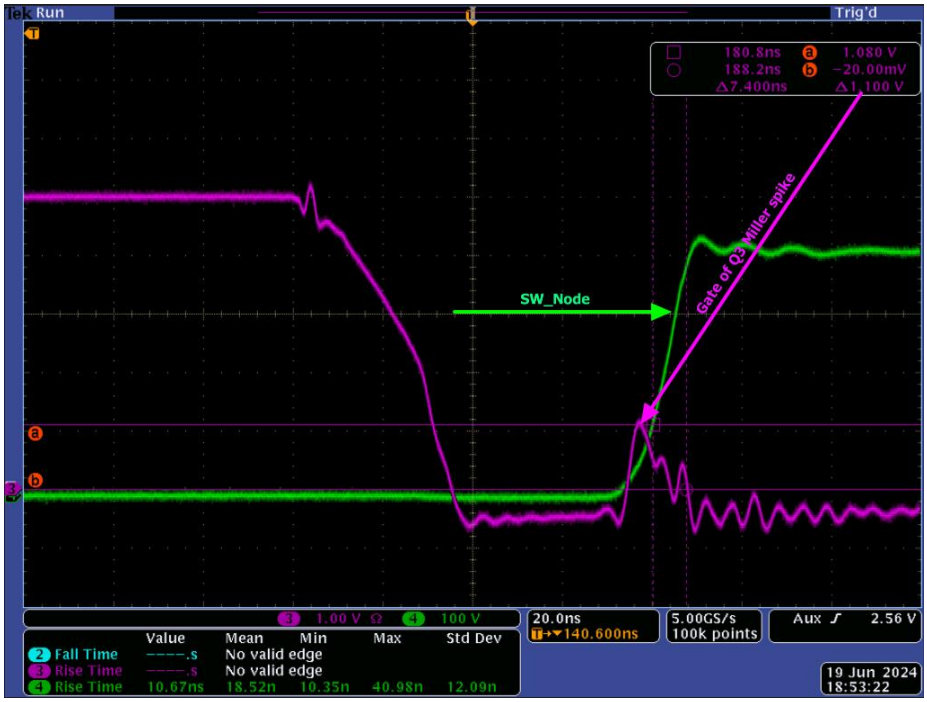

Fig. 22. Real magnitude of Miller spike taken with PMK FireFly optically isolated probe.

For Q2, the GAN080-650EBE, the gate threshold voltage is defined as a minimum 1.2 V and a maximum 2.5 V with 1.7 V being typical. This gate voltage threshold is defined as the point that the drain source current of Q2 would reach 0.037 A. By using this drive method, we have brought the Miller spike voltage to a level below the min 1.2 V. If this margin is insufficient, add the extra diode as shown in Fig. 12.

Power loss in Q2 at 400-V in, 600-W out is approximately 5 W with a Tj of 120°C. Drive power consumption ranges from 98 mA at 50 kHz to 102 mA at 200 kHz.

Conclusion

Through the use of resonant drive, the uP1964 brings the ability to tailor improved performance for GaN devices. Meanwhile, the drive voltage level can be adjusted in the uP1964 to match the GaN technology in use.

When using this approach, a "lossy" ferrite bead added for resonance reduces high-frequency ringing in the gate drive. As a result, PCB layout is less critical using this method than with standard drive techniques.

What's more there is little drawback to this approach as implementing resonant drive adds only three components which are inexpensive and small. As an added bonus, designs that employ this technique exhibit improved Miller spike immunity.

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2. "Selecting and Using Ferrite Beads for Ringing Control in Switching Converters," by Christopher Richardson and Ranjith Bramanpalli, Wurth Elektronik application note ANP025, February 15, 2015.
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4. "High-Bandwidth Isolated Voltage Measurements with Very High Common Mode Rejection Ratio for WBG Power Converters" by Pascal S. Niklaus, Reto Bonetti, Christof Stäger, Johann W. Kolar and Dominik Bortis, IEEE Open Journal of Power Electronics, September 22, 2022, pages 651-664.

About The Author

Ron Vinsant is a senior member of Technical Staff at uPI Semiconductor. With more than 30 years of experience in analog and digital power systems design, he has demonstrated success in engineering and application engineering roles at technology companies both large and small, including Vishay Siliconix, Powervation, Fairchild, Zilker Labs, SOMA Networks, Linear Tech and Teledyne. Prior to joining the power industry, he studied physics at U.C. Berkeley, Calif.

For more on designing power converters using SiC and GaN devices and related product news, see How2Power's Special Section on Silicon Carbide and Gallium Nitride Power Technology.