EOS/ESD Symposium Announces Tutorial Program

The 46th annual EOS/ESD Symposium and Exhibits, which will be held September 14-19, 2024 in Reno, NV, has introduced its 2024 tutorial & certification program. Whether you are new to ESD or have been in the industry for many years, there are tutorials and certification options for you. Find the descriptions of the tutorials in this article and use the code "TUTORIAL2024" when signing up to receive a $100 savings.

New To ESD Or Do You Need An Introduction To Base Principles?

- FC100: ESD Basics for the Program Manager
- FC101: How To's of In-Plant ESD Auditing and Evaluation Measurements

FC100: ESD Basics for the Program Manager, Saturday, September 14

Instructor: Jay Skolnik, Cofounder, Lead Engineer, Consultant, Skolnik Technical Training

This tutorial provides the foundation material for understanding electrostatics and ESD, and the role in the manufacturing and handling of ESD sensitive devices. The fundamental properties of charge, electric fields, voltage, capacitance, and current are discussed to understand key electrostatic phenomena and electrical processes. These include charge generation and decay, material properties, and induction. An overview of device failure mechanisms is presented, including how these models impact ESD control programs. Finally, the course provides an overview of ESD control procedures during handling and manufacturing and an overview of ANSI/ESD S20.20 program requirements. This full-day course is required for those in-plant auditors and program managers working toward professional ESD certification. The presentation includes many in-class demonstrations, videos, and animated slides.

Some sample topics covered in this course are:
- Definitions and relationships among important electrical and mechanical properties
- Causes of charge generation and decay
- Field effects and voltages
- Role of capacitance in ESD (Q = CV)
- Overview of key measurements including common pitfalls of some measurements
- Review of ESD failure models
- Understanding and demonstrating electrostatic induction
- Utility and limitations of air ionization
- Basic goals of ESD controls
- Properties of effective ESD control products and materials
- Overview of ANSI/ESD S20.20 ESD program development requirements

FC101: How To's of ESD Auditing and Evaluation Measurements, Sunday Sept 15

Instructor: Jay Skolnik, Cofounder, Lead Engineer, Consultant, Skolnik Technical Training

Compliance verification is one of the most important ESD program management elements, and many technical and administrative pitfalls can be avoided. The attendee will learn how to make valid auditing measurements per ESD TR53 – Compliance Verification of ESD Protective Equipment and Materials and how to recognize and avoid common pitfalls. Common instruments will be explained, and the invalid test results that can result when used incorrectly. There are many ways to administer effective compliance verification programs.

Interested In ESD Design? New Tutorials To Complete All Your ESD Training

- Introduction to On-Chip ESD Protection
- Introduction to Characterization of On-Chip ESD Protection
- Overview on ESD and Latch-up Challenges in 2.5D and 3D-Stacked ICs
- ESD Design Challenges of RF and High Speed I/Os

Introduction to On-Chip ESD Protection, Saturday, September 14

Instructor: Oliver Marichal, Chief Engineer, SOFICS

The tutorial is designed to provide a comprehensive understanding of electrostatic discharge (ESD) events and its implications on semiconductor devices. The tutorial will delve into the fundamentals of ESD, including the physics behind the electrostatic build-up and discharge processes. Integrated circuits can get damaged by ESD events during manufacturing, testing or in assembly when they are handled by people or machines. IC layout engineers can influence the robustness of their circuits by applying guidelines and tricks. Participants will explore various ESD protection strategies and design methodologies used in modern integrated circuits (ICs). The material will cover ESD devices used from basic CMOS to advanced FinFET technologies. The session will cover key topics such as on-chip ESD protection device structures and layout considerations. Through a blend of theoretical knowledge and practical examples, the tutorial aims to equip attendees with the skills necessary to understand on-chip ESD protection schemes.

This tutorial is ideal for IC engineers seeking to enhance their expertise in ESD protection for semiconductor devices.

Introduction to Characterization of On-Chip ESD Protection, Sunday, September 15

Instructor: Wim Vanhouteghem, Senior ESD Design Engineer and Head of Measurement Lab, Sofics

This course is about characterizing the Electrostatic Discharge (ESD) robustness of semiconductor circuits and protection solutions. It includes the typical measurement techniques like HBM, MM, CDM, TLP, VF-TLP, HMM, and IEC 61000-4-2 used in the industry. The material provides an overview of the advantages and disadvantages of each technique.

The tutorial will also cover the interpretation of test results. Emphasis will be placed on understanding the trade-offs and design considerations in optimizing ESD protection devices for different applications.

This tutorial is tailored for professionals in semiconductor device design and testing, seeking to deepen their expertise in ESD characterization.

Learning Outcomes:

- Understanding ESD Characterization Techniques: Learn about the various techniques and methodologies used in the characterization of ESD protection devices.
- Familiarity with ESD Test Models: Learn about different ESD test models, such as Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM), and their applications in device testing.
- Understand usage of Test Equipment: Understand the usage of specialized equipment for ESD characterization, such as Transmission Line Pulse (TLP) testing systems.
- Interpreting Test Data: Develop the ability to analyze and interpret test results to assess the performance and reliability of ESD protection structures.

Overview on ESD and Latch-up Challenges in 2.5D and 3D-Stacked ICs, Sunday, September 15

Instructors: Mirko Scholz, Principal Engineer in ESD Development, Infineon Technologies; Marko Simicic, imec

2.5D and 3D integration are commercially available packaging options in the semiconductor industry. The Industry Council on ESD targets level is working on a white paper that discusses the ESD challenges of die-to-die interfaces in 2.5D/3D stacked ICs. In this invited talk, we provide an overview of the ESD and latch-up challenges that are currently solved or need to be solved in the near future. We discuss the impact of 3D integration on the ESD and latch-up robustness. ESD testing challenges like the assessment of the CDM robustness of internal IOs are covered and the specific requirements for the ESD protection design in 2.5D/3D stacked ICs are discussed. Our talk will show that all ingredients for the successful enablement of commercial 2.5D/3D stacked ICs are ready to be used.

ESD Design Challenges of RF and High Speed I/Os, Sunday, September 15

Instructor: Dolphin Abessolo-Bidzo, Senior Principal RF ESD & Latch-Up Design Engineer, NXP Semiconductors

RF and high speed I/Os are typically very challenging to protect against ESD stresses. This is due to the very limited ESD protection capacitance load "budget" of those pins for functional reasons. Furthermore, as the advanced CMOS technology has evolved towards 5 nm FinFET and beyond, the thinner gate oxide makes the devices become more vulnerable to ESD zaps. At the same time, a trend of a 2X increase of per-pin data rate every 4 years is observed for high-speed SerDes wireline I/Os (e.g., USB, Ethernet, etc.), and higher bandwidth is required for RF I/Os of Millimeter wave Transceivers.

This presentation will cover the following topics:
- The increase of data rate and bandwidth requirement for every SerDes generation and the advanced CMOS technology gate oxide scaling related aspects
- The ESD design trade-offs and challenges of RF and High-Speed I/O's
- The examples of ESD design techniques applicable to RF and high-speed I/O's (RF ESD co-design, T-coil design, etc.)
- The lowering of CDM level for ultra-high-speed I/O interfaces (recommendation by the Industry Council on ESD Target Levels)

Ready To Implement Your Company's ESD Control Plan Or Become Certified?

- FC340: ESD Program Development and Assessment, ANSI/ESD S20.20 Seminar (Two-day course)

FC340: ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar) – Saturday-Sunday September 14-15

Instructor: David Swenson, Cofounder, Consultant, Affinity Static Control Consulting

This seminar provides instruction on designing and implementing an ESD control program based on the newest release of ANSI/ESD S20.20. The course provides participants with the tools and techniques to prepare for an ESD facility audit. This two-day course is an ESDA certification requirement for in-plant auditors and program managers who are working toward professional ESD certification.

The following topics are covered in this course:
- Overview of ANSI/ESD S20.20
- How to approach an assessment
- Administrative elements
- ESD program assessment
- ESD program techniques for different applications
- Technical elements
- Overview of the assessment process
- The audit checklist and follow-up questions

For more information on tutorials, see the website.