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Overcoming Power Challenges In Optical Transceivers With Two-Stage Buck Regulators

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Several challenges face today's network and datacenter system power designers. The increase in data rates—fueled by growth in streaming services, cloud computing, and virtual and augmented reality compounded by increased usage of artificial intelligence— translates to increased power requirements usually in the same or smaller space. Traditional methods of power conversion using buck topologies may be battle-hardened but offer little opportunity to significantly improve the efficiency and size of the converter. They also struggle to provide the performance required to support sub-10-nm loads which require very low output voltages often combined with higher currents.

In this article, we introduce the two-stage buck regulator architecture as an innovative method of achieving efficient conversion from high input to low output voltages. This novel architecture consists of a first-stage charge pump to divide the input voltage down to a lower intermediate value, followed by a second-stage buck regulator. In devices produced by pSemi, the two stages are integrated in a single, monolithic die and combine to provide a highly efficient solution for high stepdown conversion ratios.

The low-voltage, second-stage buck converter requires a smaller output inductor (than would a conventional single-stage buck) which makes the topology ideal for low-profile applications. The low-profile advantage allows the system designer to place the two-stage regulator solution on the underside of the main PCB. This placement simultaneously frees space on the topside for other critical components while also allowing the device to be placed directly under the load ASIC or DSP, thus reducing PCB routing I^2R losses. These benefits are especially helpful in in optical transceiver applications where the application of the two-stage regulator has been particularly successful.

In this article, we'll begin by reviewing the power requirements and space constraints in optical transceivers which motivate the use of the two-stage architecture. The key features of this architecture will then be described followed by a more-detailed explanation of how this architecture works and how it differs from a single-stage buck converter.

From there, we'll provide guidance on how to implement converter designs based on the two-stage regulator, using pSemi's PE24108 IC (see the reference) in the examples presented. The selection of the required inductor, output capacitor, and compensation components will be covered, including cases where regulators are paralleled for higher power. We conclude by discussing trends in the optical transceiver market which favor further use of the two-stage architecture.

PCB Real Estate Problem In Practice: Optical Transceivers

Optical transceivers are a good example of the PCB real estate problem needing a practical solution. These high-density transceivers require conversion from 3.3-V supplies to support the customer DSPs and ASICs at voltages in the range of 0.3 to 0.5 V at currents greater than 20 to 30 A. So, some type of voltage regulator solution is needed by the transceivers.

However, because their form factors are determined by an industrial standard, transceiver module manufacturers must accommodate all components in a fixed PCB area, resulting in chronic space issues. In fact, the top side of the PCB is occupied with mechanical and optical components.

Now power engineers are motivated to put voltage regulators on the backside of the PCB to free up more space on the top side, allowing a low-impedance and low-loss supply path to the main DSP or ASIC core. However, this movement introduces a height constraint issue which is typically required to be under 1.2 to 1.5 mm, forcing designers to use small inductors which can incur a significant efficiency penalty. What's more, the height restriction does not leave room for heatsinking (Fig. 1).

The two-stage buck architecture provides an ideal solution to achieve an ultra-low profile in the power conversion area with best-in-class conversion efficiency in this application.

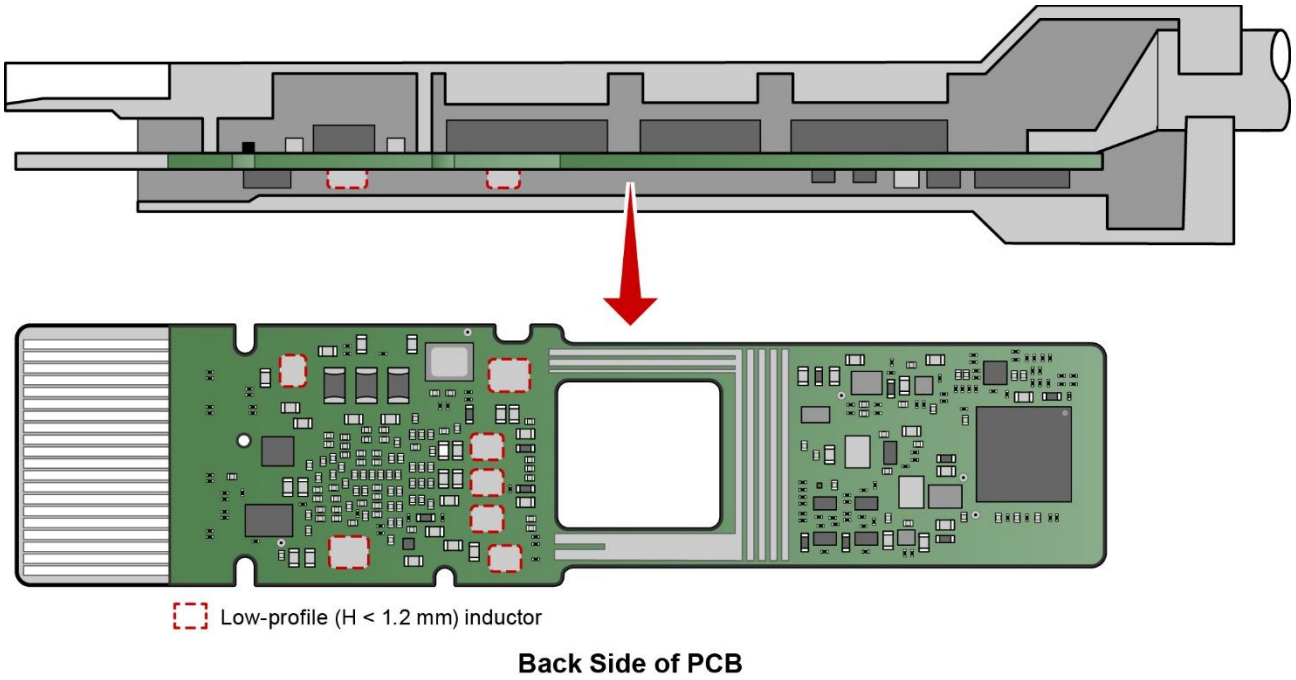


Fig. 1. Typical optical transceiver PCB.

Two-Stage Regulator Architecture Basics

Fig. 2 shows the basic outline of the two-stage architecture: a first-stage charge pump, capacitor divider followed by a second-stage buck regulator. We might think that a two-stage approach would result in lower power conversion efficiency. However, the first-stage capacitor divider is effectively considered as "lossless" or, at least, very high efficiency. The capacitor divider and the buck regulator use low-voltage FETs resulting in improved overall efficiency. The two-stage architecture is particularly effective for high-low voltage ratio conversion.

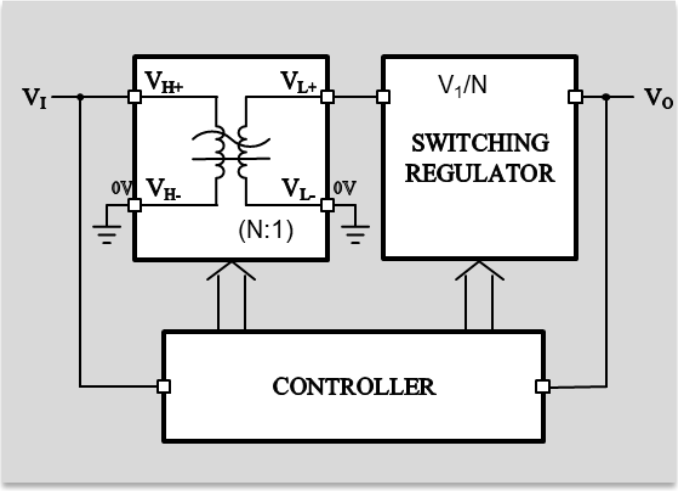
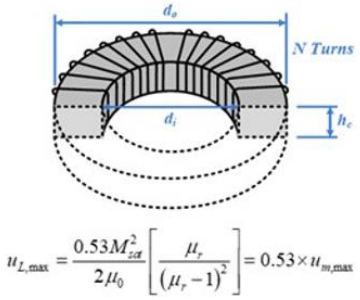
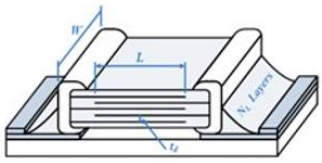


Fig. 2. The two-stage architecture—a charge pump divider followed by a buck regulator.

The key point is that most of the work is being done using capacitive energy transfer, thereby reducing the amount of work being done by the output inductor. In Fig. 3, we can see that the power storage or density of a capacitor is more than 400 times greater than the power density of an inductor. Hence, capacitive energy transfer can yield much higher energy density solutions if harnessed correctly.



$$u_{L,\max} = \frac{0.53 M_{sat}^2}{2\mu_0}\left[\frac{\mu_r}{(\mu_r - 1)^2}\right] = 0.53 \times u_{m,\max}$$



$$u_{C,\max} = \frac{U_C}{vol_C} = \frac{P_{sat}^2}{2\varepsilon_0}\left[\frac{\varepsilon_r}{(\varepsilon_r - 1)^2}\right] = u_{e,\max}$$

Structure	Material	Param 1	Param 2	Energy Density
MLCC	Thick Film $BaTiO_3$	ε_r = 3500	P_{sat} = 0.165 C/m²	439.51 μJ/mm³
Toroidal	N40 (NiZn Ferrite)	μ_r = 15	M_{sat} = 0.270 T	1.1 μJ/mm³

Capacitors have potentially 400x higher energy density compared with inductors

Fig. 3. Limitations of inductors in power conversion.

Two-Stage Architecture Deeper Dive

Consider the traditional buck converter solution in Fig. 4a. Traditional buck regulators are widely used in the industry, but there are some disadvantages.

If we consider the Vx node as the midpoint of the buck FETs, this switches between the input voltage and ground (usually a FET body diode-drop below ground). This means that the output filter, the output inductor, and capacitance must be relatively large.

In addition, the Vx node voltage further increases because the output leakage inductance causes an overshoot spike as the current reverses in the output inductor. This results in lower conversion efficiency and increased EMI. Moreover, the designer must select higher voltage FETs—again, reducing the conversion efficiency. Further, the larger inductance results in higher DCR losses and poorer transient response. In effect, the inductor is doing all the work.

In applications with a large stepdown from V_{IN} to V_{OUT}, say 12 V to 1 V or 3.3 V to 0.5 V, the upper side FET is only on for 8% or 15% of the time, respectively. During this short on-time, the converter must provide a high enough peak current to support the total average input current. This leads to high input current pulses which can result in higher EMI and the need for larger input capacitance.

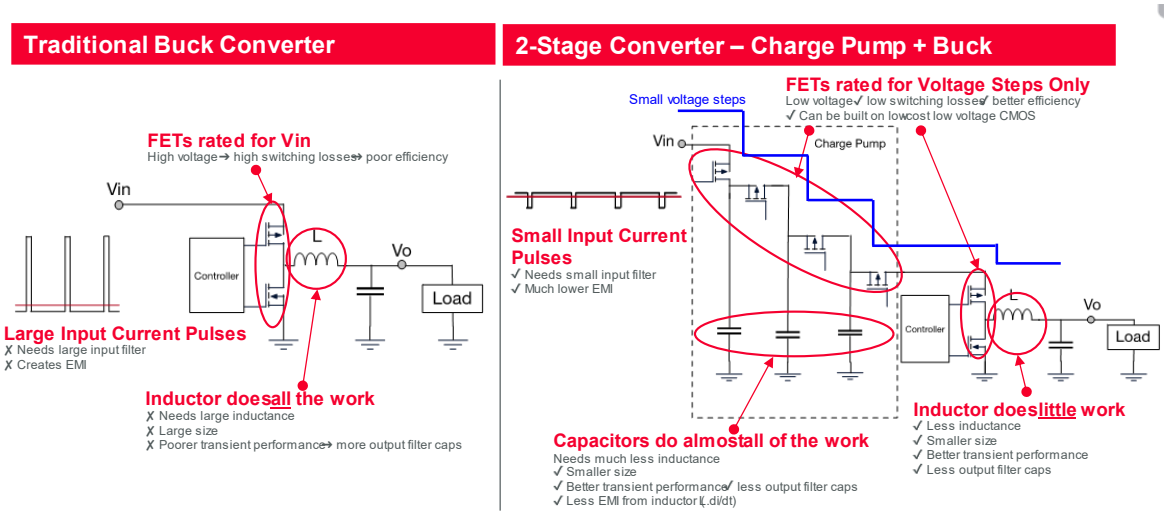


Fig. 4. A traditional buck converter (a) versus a two-stage charge pump+ buck converter (b).

Now consider Fig. 4b, the two-stage architecture. The charge pump, capacitor divider is inserted as a first stage and converts the input voltage down in linear steps. For example, in a 12-V input to 1-V output converter, we use a divide-by-3 which staircases the voltage to from 12 V to 8 V and finally to 4 V. This means that each of the charge pump FETs can be low voltage (except for the first FET which is exposed to the input voltage). The result is an extremely high conversion first-stage efficiency with capacitors doing all the work.

Now, the buck converter is only used to convert the last step, in this case from 4 V to 1 V. This allows the use of low-voltage buck FETs for further efficiency improvement. The output inductor becomes smaller as the Vx node is now slewing between a much-reduced input voltage and ground. This results in smaller, low-profile inductors with reduced reverse leakage voltage spikes that would otherwise contribute to EMI. A secondary benefit is that the operating frequency can now be increased to further reduce the inductor size, resulting in faster transient response.

The second-stage regulator now operates at larger duty cycles. This is reflected at the input of the first-stage charge pump (the input of the converter). This means that the peak to average current ratio has now been reduced, resulting in better EMI performance.

The first-stage charge pump and second-stage regulator are integrated in one monolithic IC to provide a fully integrated converter. Further, the charge pump is implemented as a dual, interleaved converter with each phase operating at approximately 50% (Fig. 5). This ensures that at any given instant, V_{IN} is always connected to the output of the charge pump. This results in significantly improved EMI and noise performance.

Similarly, the output regulator is implemented as an interleaved converter. These dual-stage implementations mean that the converter operates close to continuous input and output current resulting in fewer input and output capacitors and improved EMI.

The two-stage solution is not necessarily suited to every application. It is ideally deployed in applications that require low-height profile and high efficiency or applications that require high input voltage to output voltage ratio. While the two-stage solution adds external components versus the single-stage buck, the added cost of the extra components tends to be offset by the benefits of the architecture. For example, there are two inductors instead of one, but the two inductors will be smaller and lower cost, so not much increase there. The charge pump capacitors are additional, but their cost is somewhat offset by the savings associated with smaller input and output caps.

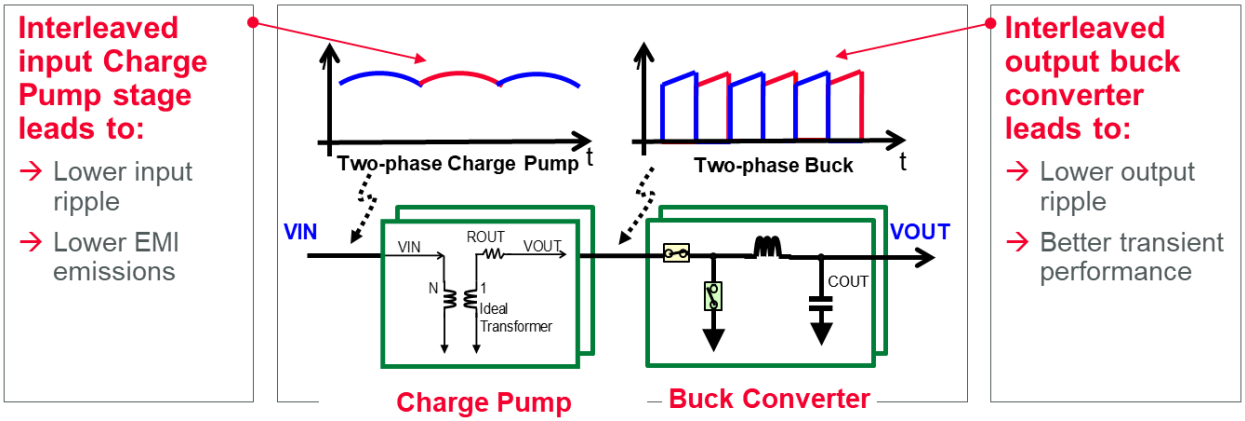


Fig. 5. The two-stage converter features interleaved input and output, resulting in lower input EMI and lower output ripple.

Practical Issues: Tips And Tricks For Power System Engineers

This section defines the components responsible for maintaining stable operation of the two-stage converter. The schematic shown in Fig. 6 highlights the key components used.

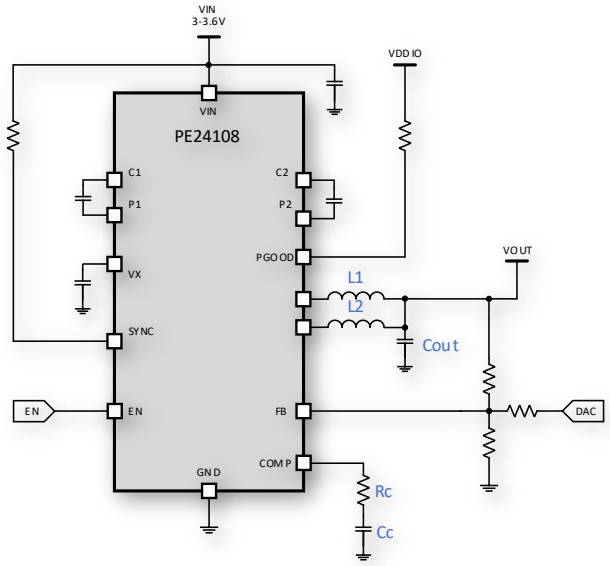


Fig. 6. Typical application schematic for the PE24108 two-stage converter.

In this example, we show a two-stage converter applied from a 3.3-V input voltage to a low output voltage in the range of 0.4 V to 0.6 V at a maximum output current of 8 A. The first-stage charge pump divides the input voltage by 2, creating an internal input voltage to the buck converter of 1.65 V nominal. The charge pump has two phases interleaved for low ripple and moderate current in each phase.

The buck converter portion operates at an 800-kHz switching frequency and has two phases, allowing lower current in each phase for smaller inductors and low ripple. The example has been optimized for efficiency, size, and performance, with recommended component values.

Inductor Selection

The output inductor value can be determined from the operating frequency, load current, ripple current, and duty cycle. The inductor should have a saturation current rating greater than the peak current limit of the device. The PE24108 two-phase interleaved buck regulator design greatly reduces the dependency on inductance such that the saturation current required through each inductor is decreased by a factor of 2. Once the input voltage, output voltage, operating frequency, and desired ripple current are known, the minimum value for the inductor can be calculated by:

$$L = \left(\frac{V_{OUT}}{\Delta I_{L(\min)} \times F_{SW}}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Some amount of ripple current is required to allow the inductor to oppose any change in current flowing through it and build up a magnetic field around the inductor to induce an opposing voltage back into the coil. Typically, ΔI_L is set to 30% of the rated output current. This is somewhat arbitrary and will determine the size of the inductor based on the frequency and output voltage required.

If the ripple current in the inductor is too low, the control loop will not have sufficient current-sense information and can be prone to instability. A smaller inductor will increase the ripple voltage but will improve the transient response. However, the peak inductor current, $I_{OUT} + \Delta I_L/2$, should be kept below the peak current limit of the device.

Using V_{IN} = 1.65 V (the value produced by the charge pump with 3.3-V nom. input), V_{OUT} = 0.5 V, F_{SW} = 800 kHz and ΔI_L equal to 3 A yields L ≈ 150 nH. The 150-nH inductors were chosen based on their low profile, current rating, and low dc resistance (6 mΩ, typ.).

Output Ripple Voltage And Output Capacitor Selection

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a source of charge for transient load conditions. Two performance characteristics to consider when selecting the value for the output capacitor are the output voltage ripple and transient response. The output voltage ripple can be approximated by using the formula:

$$Vripple = \Delta\text{VOUT (V)} = \Delta I_L \cdot \left[R_{ESR} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}}\right]$$

where, ΔV_{OUT} (V) is the amount of peak-to-peak voltage ripple at the power supply output, R_{ESR} (Ω) is the series resistance of the output capacitance, f_{SW} (Hz) is the switching frequency of the buck converter, and C_{OUT} (F) is the output total capacitance.

Note that for a multiphase converter there is output ripple current cancellation, which reduces the ripple voltage. This cancellation is a function of duty cycle due to the apparent overlap of the two ripple current phases. For a two-phase buck converter, this reduction is calculated as (D = duty cycle):

$$\text{Iripple}_{2\text{phase}} = \Delta I_L \cdot \left[\frac{1 - 2D}{1 - D}\right]$$

So, the ripple is greatest at close to D = 0 and D = 1 and is minimal at D = 0.5. In practice there will be some ripple at D = 0.5, not zero as indicated by the formula. For a typical PE24108 circuit example, with V_{IN} = 3.3 V (Vx = 1.62 V) and V_{OUT} = 0.5 V, the result would be 0.55, or a 45% reduction in ripple.

The amount of output ripple that can be tolerated is application-specific; however, a general recommendation is to keep the output ripple less than 1% of the rated output voltage. The Murata GRM188D70E476ME01D 47-µF ceramic capacitors were chosen based on their size, low output voltage and very low ESR. Using C_{OUT} = 188 µF, F_{SW} = 800 kHz, R_{ESR} = 1.25 mΩ and ΔI_L = 3 A yields Vripple = 6.2 mVpp*0.55 or 3.4 mVpp. Actual ripple will be slightly larger due to device derating and board parasitics. Fig. 7 shows a ripple measurement for this case which is slightly larger than calculated (soldered cable probe, ac coupled).

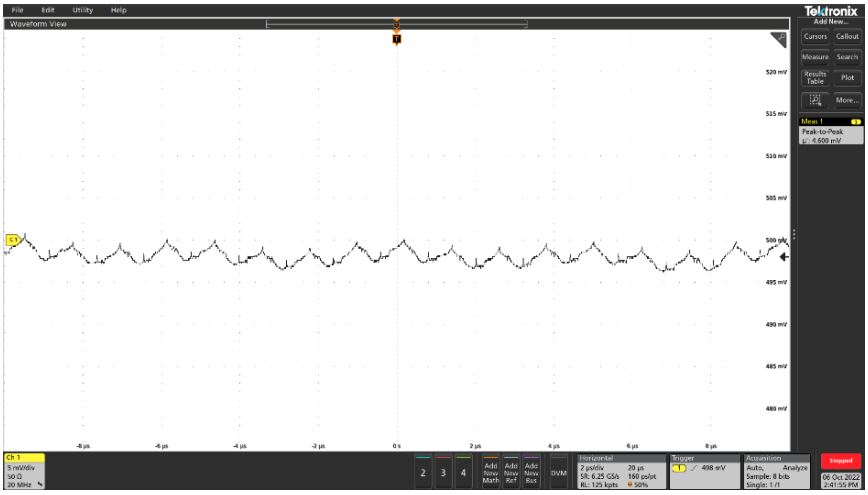


Fig. 7. PE24108 output ripple for V_{IN} = 3.3 V, V_{OUT} = 0.5 V and 8-A load. Measured ripple is 4.6 mV p-p.

Loop Compensation

The purpose of loop compensation is to meet static and dynamic performance requirements while maintaining adequate stability. Optimal loop compensation depends on the output capacitor, inductor, load, and the device itself. The table gives values for the compensation network that will result in a stable system when using 4 x 47-µF, ceramic X7T output capacitors and 150-nH inductors.

Table. Recommended compensation for the PE24108 using C_{OUT} = 4 x 47 µF and L1 = L2 = 150 nH at f_{SW} = 800 kHz.

V_{IN} (V)	V_{OUT} (V)	R_C (kΩ)	C_C (nF)
3.3	0.4	2.4	4.7
3.3	0.5	2.7	4.7
3.3	0.6	3.6	4.7
3.3	0.7	4.7	4.7
3.3	0.8	5.6	4.7
3.3	0.9	6.2	4.7
3.3	1.0	6.8	4.7

For stability purposes, it is desirable to have the slope of the gain curve at the crossover point with a value of -20 dB/decade. Phase margins of 45 degrees to 60 degrees are considered safe values that yield a well-damped load transient response.

For this application, the compensation values were adjusted to provide phase margins of 60 degrees at room temperature. Fig. 8 shows the resulting gain-phase diagram for the PE24108 operating at V_{IN} = 3.3 V, V_{OUT} = 0.5 V, I_{LOAD} = 8 A, F_{SW} = 800 kHz and T_a = 25°C.

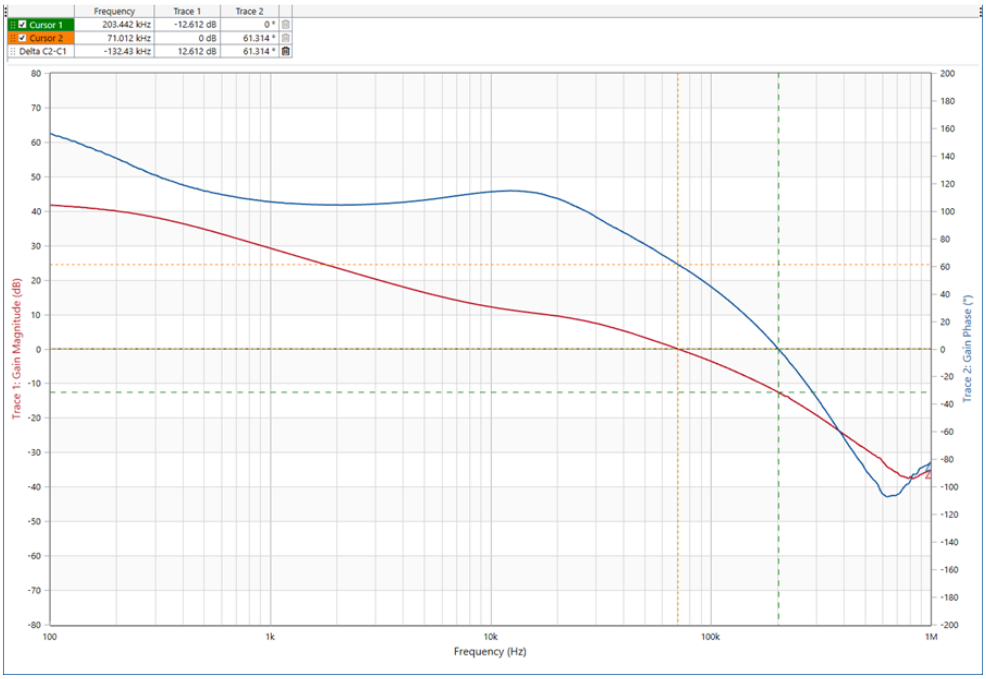


Fig. 8. Bode plot for a PE24108-based converter operating at V_{IN} = 3.3 V, V_{OUT} = 0.5 V and 8-A load.

Load Transient

The output capacitor selection will also affect the output voltage droop during a load transient. The peak droop on the output voltage during a load transient is dependent on many factors; however, the equation below can provide a reasonable estimate of the load current transient based on the ceramic output capacitance and the converter's bandwidth.

In many cases, this calculated capacitance value can be significantly larger than that required for a low steady-state ripple voltage. Note that capacitors with high ESR may increase the resulting peak transient voltage. The low ESR of the Murata output capacitors can be ignored.

$$Vtransient = \frac{Istep}{2\pi f_{BW} \cdot Cout}$$

For example, using a current step of 2 A, a converter bandwidth of 71 kHz and C_{OUT} = 188 µF yields an estimated deviation of 24 mV (Fig. 9).

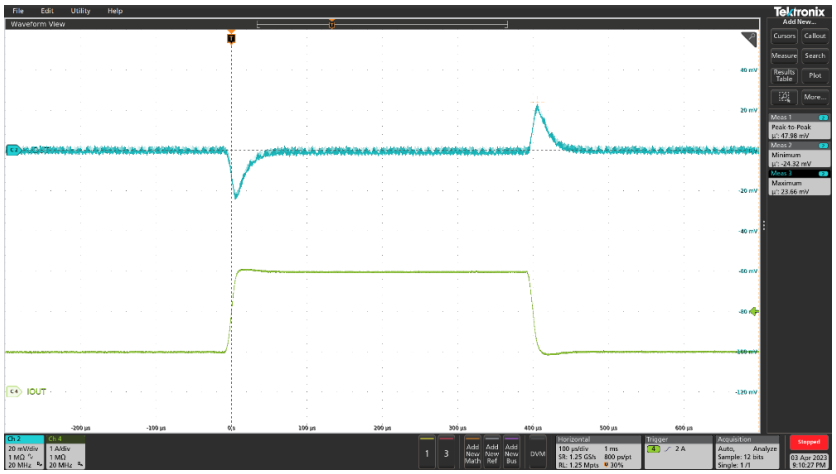


Fig. 9. Load transient for a PE24108-based converter operating at V_{IN} = 3.3 V, V_{OUT} = 0.5 V, and 1-A to 3-A load step at 0.2 A/µs.

Paralleling Devices For High Current Output

The PE24108 two-stage regulator includes functionality for paralleling devices for higher load current. A maximum of four devices may be paralleled with load capability up to 36 A. The SYNC, COMP, FB and PGOOD and EN pins of all devices should be connected. For two or more devices operating in parallel, the main feedback operating mode is referred to as master-master mode.

Master-master mode provides for each device to be a master with feedback control done individually. Each device will have a common connection to the feedback divider and the compensation R-C network on their COMP pin. The compensation R-C values are identical for all devices and are the same as for single-device operation (Fig. 10).

All devices operate from a common FB node and the feedback amplifiers drive the COMP pin, essentially averaging the feedback for all devices. The output voltage can be adjusted using a single DAC externally feeding a current via a resistor into the feedback network.

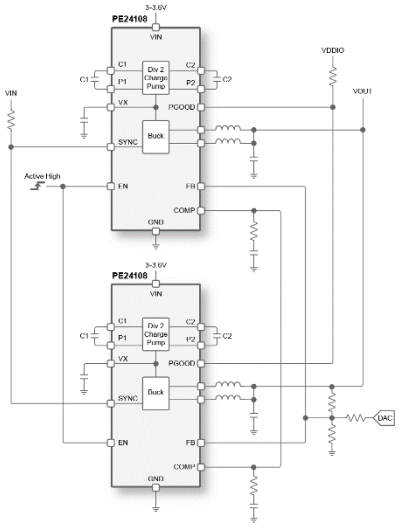


Fig. 10. Two PE24108 parts in parallel. Note that the feedback pins are tied together and the same values of R-C components are connected to each compensation pin.

For the master-master mode with all FB pins tied together, we can alternatively use a single set of R-C compensation components. The values are scaled according to the number of parallel devices.

Real-Life Applications

Again, as an example, optical transceiver modules are widely used for datacenter or telecom interconnection. They are pluggable modules in various form factors and configurations determined by the IEEE 802-3 standard. Market trends are going to smaller form factors such as CFP (centum form-factor pluggable) and QSFP (quad small form-factor pluggable), resulting in reduced space inside of the module (Fig. 11). This is the main reason why power conversion will be forced to the backside of the PCB where low profile 1.2- to 1.5-mm solutions are required.

In addition, movement to higher transmission rates (100 Gbits, 400 Gbits, and 800 Gbits) requires more powerful DSPs and ASICs with lowering core voltage 0.3 V to 0.5 V, following process-node evolution. This leads to another challenge for voltage conversion even with a 3.3-V input rail due to the very low duty cycle of <10% (in the case of a conventional buck converter as in Fig. 4a) and also use of a thin, low-profile inductor. Unfortunately, the IEEE standard does also govern the module power consumption, thus even 0.1% efficiency drop cannot be ignored.

The PE24108 two-stage regulator can enable power conversion on the backside of the PCB without sacrificing efficiency by minimizing dependency on the inductor and instead using capacitors for most of the power conversion. Backside implementation also allows a low-impedance and low-loss power path to the core rail by sitting closer to DSPs and ASICs.

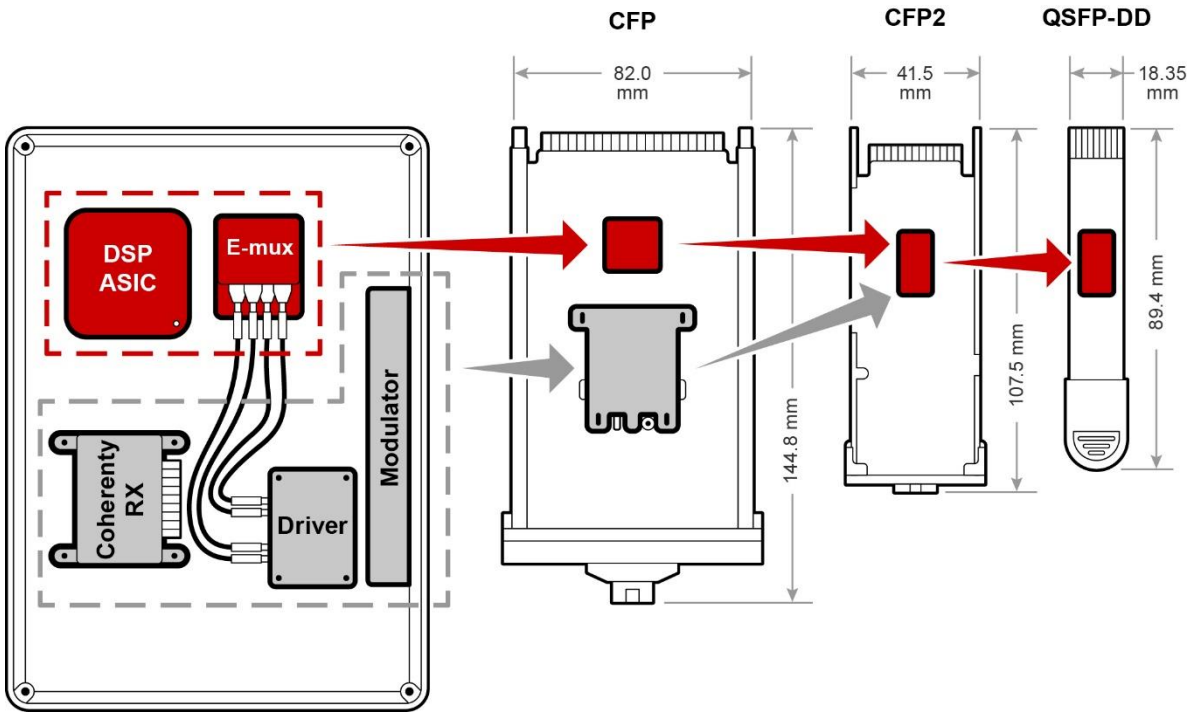


Fig. 11. Evolution of optical networks.

Reference

PE24108 datasheet.

About The Authors

Laurence McGarry is the director of marketing and systems applications for pSemi Power Products. He has over 35 years of experience in power systems and power semiconductor applications. Laurence holds a Beng Hons in electrical and electronics engineering from Glasgow University and an MBA from Washington State University.

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Kubo Tatsuya is the product manager for Murata's high efficiency buck regulator and charge pump portfolios. He has been with Murata for 23 years and has contributed to the power business in design and marketing roles. Kubo has a bachelor's degree in electrical and electronic engineering from Ritsumeikan University in Japan.

For further reading on designing dc-dc converters, see the How2Power Design Guide, locate the "Power Supply Function" category and select "DC-DC converters".