ISSUE: November 2024

Output Filter Capacitor Size Depends On Inductor Value

by Gregory Mirsky, Design Engineer, Deer Park, Ill.

In switched mode power supplies (SMPSs), the output filter capacitor—and often there are multiple capacitors—is the bulkiest component since it has to conduct significant ripple current and thus dissipate noticeable power. High power dissipation requires substantial component area to avoid capacitor overheating.

In many cases electrolytic capacitors are still being used thanks to their high reliability and low cost-per-capacitance ratio. The output filter capacitors significantly reduce the current ripple through the load by bypassing it to the return/ground path.

Typically, in an SMPS, the value of output filter capacitance is calculated based on the desired output ripple voltage and the assumed ripple current for a given inductor under the given set of operating conditions. However, this approach ignores the interplay between the capacitor and inductor in filtering the ripple current. What results is a non-optimum capacitor selection, both in terms of capacitance value and capacitor size.

In this article we will define both the electrical and physical sizes required of a capacitor used for filtering the current ripple in a converter and decide whether this capacitor can handle the ripple current while working in the output filter. To do this, we'll analyze operation of the output filter components in a simple buck converter power stage. However, the results can also be applied to other buck or bridge topologies that employ output filters.

Output Filter Role In A Converter

Consider the buck converter power stage pictured in the figure.

We will consider the schematic operation in two states:

State #1—switch SW is on, power supply creates voltage VDD at the switch SW input, which transfers current to the inductor Lc and Rload. This current has two components: the ac component charges and discharges capacitor Cf, while the dc component and unfiltered part of the ac component go to the load Rload.

State #2—switch SW is off, energy stored in inductor Lc keeps supplying the load through the diode D1.

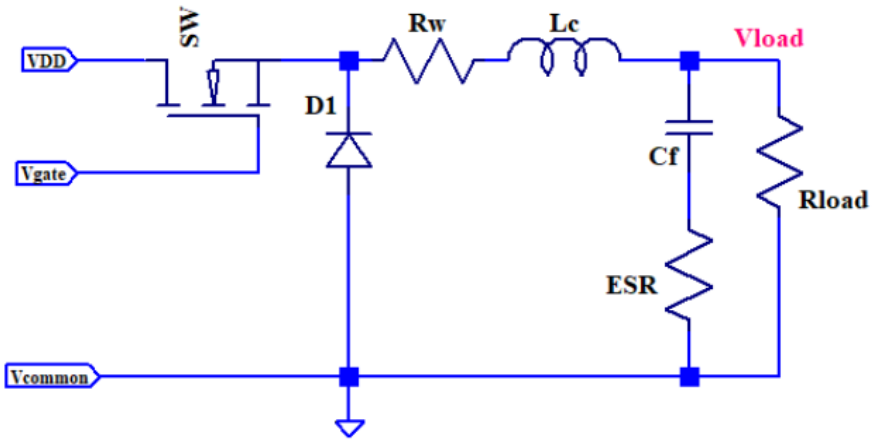

Figure. This abridged schematic of a buck converter shows the crucial components that are considered in determining the output filter capacitor requirements.

In analyzing the operation of this buck converter stage, we'll assume the following conditions:

- Switch SW is a MOSFET having channel resistance of R_{DS} in the on state and approaches infinity in the off state.
- Diode D1 may be a diode or MOSFET having voltage drop of V_{D1} when conducting and does not conduct current when off.
- Inductor Lc has a winding resistance of R_w.
- Capacitor Cf is an electrolytic capacitor having ESR much lower than the load resistance Rload. This means the whole ac current flows through the capacitor only. This facilitates the analysis.
- Cf may be a ceramic capacitor or a composition of a few types of capacitors having different values.
- When the switch SW is off, the energy stored in the inductor Lc and capacitor Cf is used to power the load.

Converter Electrical Analysis

SW Is ON—Energy Transfer And Storage Cycle:

When the switch In Fig. 1 is on, from KVL, we can write

$$V_{DD} = V_{RDS} + V_{Rw} + V_{Lc} + V_{load} \quad (1)$$

From the definition of inductor voltage, we can express V_{Lc} in terms of current

$$V_{Lc} = Lc \cdot \frac{\Delta I_{ON}}{\Delta t_{ON}} \quad (2)$$

so that we can re-write equation (1) as

$$V_{DD} = V_{RDS} + V_{Rw} + Lc \cdot \frac{\Delta I_{ON}}{\Delta t_{ON}} + V_{load} \quad (3)$$

Then, from (3), we can define ΔI_{ON} as

$$\Delta I_{ON} = \frac{\Delta t_{ON} \cdot (-V_{Rw} + V_{DD} - V_{RDS} - V_{load})}{Lc} \quad (4)$$

SW Is OFF—Energy Release Cycle

When the switch in the figure is off, and the inductor is supplying energy to the load, from KVL we can write

$$0 = V_{D1} + V_{Rw} - V_{Lc} + V_{cf} + V_{ESR} \quad (5)$$

Once again, we can express the inductor voltage in terms of its current,

$$V_{Lc} = Lc \cdot \frac{\Delta I_{OFF}}{\Delta t_{OFF}} \quad (6)$$

Plugging this definition of V_{Lc} into (5) we get

$$0 = V_{D1} + V_{Rw} - Lc \cdot \frac{\Delta I_{OFF}}{\Delta t_{OFF}} + V_{cf} + V_{ESR} \quad (7)$$

Then, solving (7) with respect to ΔI_{OFF} yields

$$\Delta I_{OFF} = \frac{\Delta t_{OFF} \cdot (V_{D1} + V_{Cf} + V_{Rw} + V_{ESR})}{Lc} \quad (8)$$

Since the inductor current cannot interrupt,

$$\Delta I_{ON} = \Delta I_{OFF}$$

Substituting the expressions from equations (4) and (8) we obtain

$$\frac{\Delta t_{ON} \cdot (-V_{Rw} + V_{DD} - V_{RDS} - V_{load})}{Lc} = \frac{\Delta t_{OFF} \cdot (V_{D1} + V_{Cf} + V_{Rw} + V_{ESR})}{Lc}$$

or

$$\Delta t_{ON} \cdot (-V_{Rw} + V_{DD} - V_{RDS} - V_{load}) = \Delta t_{OFF} \cdot (V_{D1} + V_{Cf} + V_{Rw} + V_{ESR}) \quad (9)$$

Assuming the switching period is T_{SW} and designating the duty-cycle as

$$D_c = \frac{\Delta t_{ON}}{T_{SW}}$$

and recollecting that the switching frequency

$$f_{SW} = \frac{1}{T_{SW}}$$

yields

$$D_c = \Delta t_{ON} \cdot f_{SW}$$

Having that definition of Dc, we can express Δt_{OFF} in terms of Dc:

$$\Delta t_{OFF} = T_{SW} - \Delta t_{ON} = T_{SW} - T_{SW} \cdot D_c = T_{SW} \cdot (1 - D_c) = \frac{1 - D_c}{f_{SW}} \quad (10)$$

Therefore, (9) becomes

$$\frac{D_c}{f_{SW}} \cdot (-V_{Rw} + V_{DD} - V_{RDS} - V_{load}) = \frac{1 - D_c}{f_{SW}} \cdot (V_{D1} + V_{Cf} + V_{Rw} + V_{ESR})$$

or

$$D_c \cdot (-V_{Rw} + V_{DD} - V_{RDS} - V_{load}) = (1 - D_c) \cdot (V_{D1} + V_{Cf} + V_{Rw} + V_{ESR}) \quad (11)$$

Solving for D_c, we get

$$D_c = \frac{V_{D1} + V_{Cf} + V_{Rw} + V_{ESR}}{V_{D1} + V_{DD} + V_{Cf} - V_{RDS} + V_{ESR} - V_{LOAD}} \quad (12)$$

Now, we can decide what ripple current is acceptable for the load, using (4) or (8), the expressions for ΔI_{ON} and ΔI_{OFF}, respectively. Let's use (8).

Assuming ripple current swing to be the γ_{ripple} portion of the dc current

$$\frac{(1 - D_c)(V_{D1} + V_{Cf} + V_{Rw} + V_{ESR})}{f_{SW} \cdot Lc} = \gamma_{ripple} \cdot \frac{P_{out}}{V_{load}} \quad (13)$$

Hence the inductor value is

$$Lc = \frac{V_{load} \cdot (D_c - 1)(V_{D1} + V_{Cf} + V_{Rw} + V_{ESR})}{P_{out} \cdot f_{SW} \cdot \gamma_{ripple}}$$

This inductor should work in a continuously conducting mode at the minimum duty cycle D_{c_min}:

$$Lc = \frac{V_{load} \cdot (D_{c\_min} - 1)(V_{D1} + V_{Cf} + V_{Rw} + V_{ESR})}{P_{out} \cdot f_{SW} \cdot \gamma_{ripple}} \quad (14)$$

Current that warms up the capacitor is the RMS value of the ripple current, which in case of a triangular current shape is:

$$I_{rpl\_rms} = \frac{\Delta I_{ON}}{\sqrt{3}} + \frac{\Delta I_{OFF}}{\sqrt{3}} = \frac{2}{\sqrt{3}} \cdot \Delta I$$

This current RMS value in a continuous-conduction mode is acting for the whole period of the converter operation, which is

$$T_{SW} = \frac{1}{f_{SW}}$$

This ripple current causes the capacitor to warm up due to power dissipated by the resistive structures of the capacitor. These resistive structures make up the equivalent series resistance (ESR) of the capacitor, which can be expressed as tangent of loss angle—tan(δ), which comes from the datasheet. This tangent of loss angle is a tangent of the angle between the vector denoting the capacitor reactance and full impedance, created by the series connection of ESR and reactance.

Therefore, since the modulus of the capacitor Cf reactance at frequency ω (ω =2*π*f_{SW}) is

$$X_C = \frac{1}{\omega \cdot Cf} \quad (15)$$

$$\tan \delta = \frac{ESR}{X_C} \quad (16)$$

and

$$ESR = X_C \cdot \tan \delta \quad (17)$$

Power loss in the ESR is

$$P_{loss} = (I_{rpl\_rms})^2 \cdot ESR = (I_{rpl\_rms})^2 \cdot X_C \cdot \tan \delta = \frac{(\Delta I_{ON})^2}{3} \cdot \frac{1}{\omega \cdot Cf} \cdot \tan \delta \quad (18)$$

Power loss in a capacitor causes its temperature rise, which may be averse to the capacitor and thus limited by specification. Power is being dissipated by the capacitor housing while the capacitor is working. So the power dissipating ability of a capacitor depends on the size of the capacitor body dissipating area (denoted simply as Area), temperature rise of the capacitor body ΔT, and material the capacitor is made from, which is expressed by the material dissipation factor β.

$$P_{loss} = \beta \cdot Area \cdot \Delta T \quad (19)$$

Equating (18) and (19), we can find the allowed current ripple through a capacitor provided the allowable temperature rise ΔT and capacitor size (Area) are given, or the filter capacitor Cf capacitance, necessary for filtering out the current ripple ΔI_{ON}.

$$\frac{(\Delta I_{ON})^2}{3} \cdot \frac{1}{\omega \cdot Cf} \cdot \tan\delta = \beta \cdot Area \cdot \Delta T \quad (20)$$

Plugging in (4) for ΔI_{ON}, we can get the marginal value for the Lc

$$\frac{\left[\frac{\Delta t_{ON} \cdot (-V_{Rw} + V_{DD} - V_{RDS} - V_{load})}{Lc}\right]^2}{3} \cdot \frac{1}{\omega \cdot Cf} \cdot \tan\delta = \beta \cdot Area \cdot \Delta T \quad (21)$$

Denoting the duty-cycle as Dc and switching frequency as f_{SW}, we get

$$D_c = \Delta t_{ON} \cdot f_{SW} \qquad \Delta t_{ON} = \frac{D_c}{f_{SW}} \quad (22)$$

$$Lc = \frac{V_{load} \cdot (D_{c\_min} - 1)(V_{D1} + V_{Cf} + V_{Rw} + V_{ESR})}{P_{out} \cdot f_{SW} \cdot \gamma_{ripple}} \quad (23)$$

And solving (18) for Cf, we obtain

$$Cf = \frac{D_c^2 \cdot \tan\delta \cdot (V_{load} - V_{DD} + -V_{Rw} + V_{RDS})^2}{3 \cdot Lc^2 \cdot (\beta \cdot Area \cdot \Delta T) \cdot \omega \cdot f_{SW}^2} \quad (24)$$

Design Example

To illustrate the application of the above equations, we'll assume the following values for an example power stage design.

f_{SW} = 240 kHz

$\omega = 2\pi \bullet f_{SW}$

P_{out} = 124 W

V_{DD} = 48 V

γ_{ripple} = 0.015

V_{load} = 12 V

$I_{in} = P_{out}/V_{DD}$

ΔT = 10 K

V_{D1} = 0.65 V

β = 13 W/K•m^2

$D_{c\_min} = V_{load}/V_{DD}$ = 0.25

Rw = 12 x 10^{-3} Ω

R_{DS} = 27 x 10^{-3} Ω

V_{ESR} = 0.1 V

V_{cf} = Vload – V_{ESR} = 11.9 V

V_{RDS} = R_{DS}•I_{in}

Area = 5.498 x 10^{-4} m^2

tan δ = 0.15

VRw = Rw• (P_{out}/V_{load}) = 0.124 V

Dc = 0.94

Plugging in values from above intro equation 23 yields the following result for Lc:

$$Lc = \frac{V_{load}\cdot\left(D_{c_{min}}-1\right)(V_{D1}+V_{Cf}+V_{Rw}+V_{ESR})}{P_{out}\cdot f_{SW}\cdot\gamma_{ripple}} = 257.54 \text{ x } 10^{-6} \text{ H}$$

Accounting for a design margin of about 20% and then choosing the next available standard value, we settle on an inductance of

Lc = 330 µH

With that as the inductance, we can use equation (24) to calculate Cf.

$$Cf = \frac{D_c{}^2\cdot\tan\delta\cdot(V_{load}-V_{DD}+-V_{Rw}+V_{RDS})^2}{3\cdot Lc^2\cdot(\beta\cdot Area\cdot\Delta T)\cdot\omega\cdot f_{SW}{}^2} = 83.783 \text{ x } 10^{-9} \text{ F}$$

In this case, use of an electrolytic capacitor is preferable cost wise and because it avoids the decay in capacitance with dc offset, which is a problem with ceramic capacitors. We select a value of

$$Cf = 10\ \mu F$$

as that is the best fit in terms of cost, size and performance.

Determining Adequate Filter Capacitor Size

Capacitor reactance:

$$Z_C = \frac{1}{\omega\cdot Cf}$$

$$P_{AC} = I_{rip}{}^2\cdot Z_C$$

where P_{AC} represents the power generated by the capacitor reactance. Due to the imperfectness of the insulator, there are usually losses defined by the loss angle δ. These losses are active and generate heat. The resistance equivalent that generates this heat is the ESR.

$$P_{loss} = P_{AC}\cdot\tan\delta$$

$$P_{loss} = \left(I_{rip}\right)^2\cdot Z_C\cdot\tan\delta$$

$$P_{loss} = \left(I_{rip}\right)^2\cdot Z_C\cdot\left[\frac{\tan\delta}{(\omega\cdot Cf)}+R_{leads}\right]$$

$$P_{loss} = \beta\cdot Area\cdot\Delta T$$

$$\Delta T = \frac{I_{rip}{}^2 \cdot \left(R_{leads} + \frac{\tan\delta}{Cf \cdot \omega}\right)}{Area \cdot \beta}$$

where ΔT = temperature rise and β = material dissipation coefficient, which for aluminum is equal to 13 W/(K•m^2)

$Area = \frac{\pi}{\Lambda} \cdot D \cdot (D + 4 \cdot Length)$

which represents the capacitor's power dissipating area.

$$\Delta T = \frac{I_{rip}{}^2 \cdot \left(R_{leads} + \frac{\tan\delta}{Cf \cdot \omega}\right)}{Area \cdot \beta}$$

$I_{rip} = \sqrt{\frac{Area \cdot Cf \cdot \beta \cdot \omega \cdot \Delta T}{\tan\delta + (Cf \cdot R_{leads} \cdot \omega + 1)}}$ which is an RMS value of the ripple current because it creates heat in the capacitor.

As $ESR = \frac{\tan\delta}{Cf \cdot \omega}$, we can write

$$I_{rip} = \sqrt{\frac{Area \cdot \beta \cdot \Delta T}{ESR + \left(R_{leads} + \frac{1}{Cf \cdot \omega}\right)}}$$

The ripple current in the inductor, incorporated into converters, is triangular. So

$$I_{rpl} = \frac{I_{rpl\_max}}{\sqrt{3}}$$

Therefore

$$I_{rip\_max} = \sqrt{3} \cdot \sqrt{\frac{Area \cdot \beta \cdot \Delta T}{ESR + \left(R_{leads} + \frac{1}{Cf \cdot \omega}\right)}}$$

$$\Delta I_{rip} = \frac{\sqrt{3}}{2} \cdot \sqrt{\frac{Area \cdot \beta \cdot \Delta T}{ESR + \left(R_{leads} + \frac{1}{Cf \cdot \omega}\right)}}$$

Example:

tan δ = 0.15

D= 20 mm

Length = 35 mm

which represent the capacitor's dimensions, chosen arbitrarily in this example, but which must be selected from a manufacturer's database.

$$ESR = \frac{\tan\delta}{Cf \cdot \omega} = 9.947 \text{ x } 10^{-3}$$

1 mΩ = 0.001 Ω

R_{leads} = 25 mΩ

The current this capacitor can handle based on its dimensions is

$$I_{rip} = \sqrt{\frac{Area \cdot \beta \cdot \Delta T}{ESR + \left(R_{leads} + \frac{1}{Cf \cdot \omega}\right)}} = 1.796\ A$$

$$\Delta I_{rip} = \frac{\sqrt{3}}{2} \cdot \sqrt{\frac{Area \cdot \beta \cdot \Delta T}{ESR + \left(R_{leads} + \frac{1}{Cf \cdot \omega}\right)}} = 1.556\ A$$

If one capacitor in unable to handle this current, two or more in parallel will do this job. Each capacitor may have just a half or quarter of the total capacitance.

This article shows that an output filter capacitor(s) should not be selected arbitrarily since they interact with the converter's inductor.

About The Author

Gregory Mirsky is a design engineer working in Deer Park, Ill. He currently performs design verification on various projects, designs and implements new methods of electronic circuit analysis, and runs workshops on MathCAD 15 usage for circuit design and verification. He obtained a Ph.D. degree in physics and mathematics from the Moscow State Pedagogical University, Russia. During his graduate work, Gregory designed hardware for the high-resolution spectrometer for research of highly compensated semiconductors and high-temperature superconductors. He also holds an MS degree from the Baltic State Technical University, St. Petersburg, Russia where he majored in missile and aircraft electronic systems.

Gregory holds numerous patents and publications in technical and scientific magazines in Great Britain, Russia and the United States. Outside of work, Gregory's hobby is traveling, which is associated with his wife's business as a tour operator, and he publishes movies and pictures about his travels online.