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Current Mode-Controlled DC-DC Regulators (Part 1): A Review Of Small-Signal Behavior

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With simple operation and dynamics, current-mode control requires two loops: a wide-bandwidth inner current loop and an outer voltage regulation loop. Commonly used forms of current-mode control[1-3] include peak, valley, average, hysteretic, constant on-time, constant off-time and emulated. Each technique offers certain advantages and trade-offs depending on the design requirements.

This article, part one of a multipart series, represents an update to a previous series I wrote in 2014[3] with more focus on the inner current loop. This part lays the groundwork for a subsequent article that details a cohesive implementation for a constant-current constant-voltage (CC-CV) circuit with two loops using a shared network for compensation.

Part 1 begins with an overview of the small-signal behavior in fixed-frequency, naturally sampled, peak current-mode, pulse-width modulated (PWM) dc-dc regulators. Following a brief review of the operating principles of peak and valley current-mode architectures, I'll review the small-signal behavior of the inner current loop and outer voltage loop, including relevant considerations for slope compensation.

If you're primarily interested in loop compensation design, part 2 of this series will offer an example using a commercially available two-phase synchronous buck controller. This example will illustrate a procedure to select components for the compensation network.

Current-Mode Control Techniques

Among the various forms of current-mode control, the most popular is peak current-mode control (PCMC) with slope compensation,[4] coinciding with its broad adoption by power-management integrated circuit (IC) manufacturers and power-supply vendors. The main factors contributing to the ubiquity of PCMC are its straightforward compensation, inherent cycle-by-cycle overcurrent protection, automatic input-voltage feedforward, and easier implementation of current sharing for multiphase scalability (also known as "stackability"). PCMC's shortcomings are current-loop noise sensitivity and a limitation of the switch minimum on-time, particularly in nonisolated applications that require a high voltage-step-down ratio from input to output.

The emulated peak current-mode control (EPCMC) architecture[2, 5] partially eases these shortcomings, although the sampling time of the valley inductor current during the PWM off-time restricts the maximum duty cycle. Valley current-mode control (VCMC), on the other hand, has poor line feedforward characteristics and different requirements for slope compensation.

Average current-mode control (ACMC) uses the inductor current waveform and an additional gain and integration stage before comparing the signal to a voltage-ramp waveform, similar to voltage-mode control. Apropos of its high current-loop gain, ACMC is often used for current-source-type applications such as battery charging, supercapacitor charging and LED lighting. Also used in automotive dual-battery (12 V and 48 V) systems that require bidirectional current control with buck or boost operating modes,[6] ACMC benefits from better noise immunity and improved operation in light-load discontinuous conduction mode while sidestepping the slope compensation requirement. However, the need to compensate two loops hinders a broader adoption of this technique, internal compensation techniques notwithstanding.

As another option, hysteretic-mode control offers excellent transient response, but the switching frequency varies across both line and load to maintain regulation. That makes electromagnetic interference (EMI) filter design more difficult. Semi-hysteretic techniques such as constant on-time (COT) control offer a quasi-constant switching frequency, albeit with possible duty-cycle jitter and an inability to stack phases.

The table captures various current-mode techniques and lists commercially available current-mode controller ICs from Texas Instruments (TI).

Table. Current-mode control techniques and dc-dc controller examples.

Control technique	PCMC	EPCMC	PCMC + VCMC	ACMC	COT
TI controller IC	LM5137(F)[4]	LM5117[5]	LM5176[7]	LM5171[6]	LM5085[2]
Power-stage topology	Buck	Buck	Noninverting buck-boost	Bidirectional buck-boost	Buck

A Brief Review Of PCMC And VCMC

The circuit diagrams in Fig. 1 represent those for peak current-mode boost and valley current-mode buck stages operating in continuous conduction mode (CCM) at a fixed switching frequency with duty cycle, *D*. Fig. 1 explicitly denotes parasitic elements for the inductor dc resistance (DCR) and output capacitor equivalent series resistance (ESR). The current sensor in Fig. 1 is ground referenced and located in series with the low-side switch. Of course, PCMC is much more common than VCMC, especially as PCMC offers inherent cycle-by-cycle overcurrent protection, multiphase capability and transformer volt-second balancing in isolated circuits.

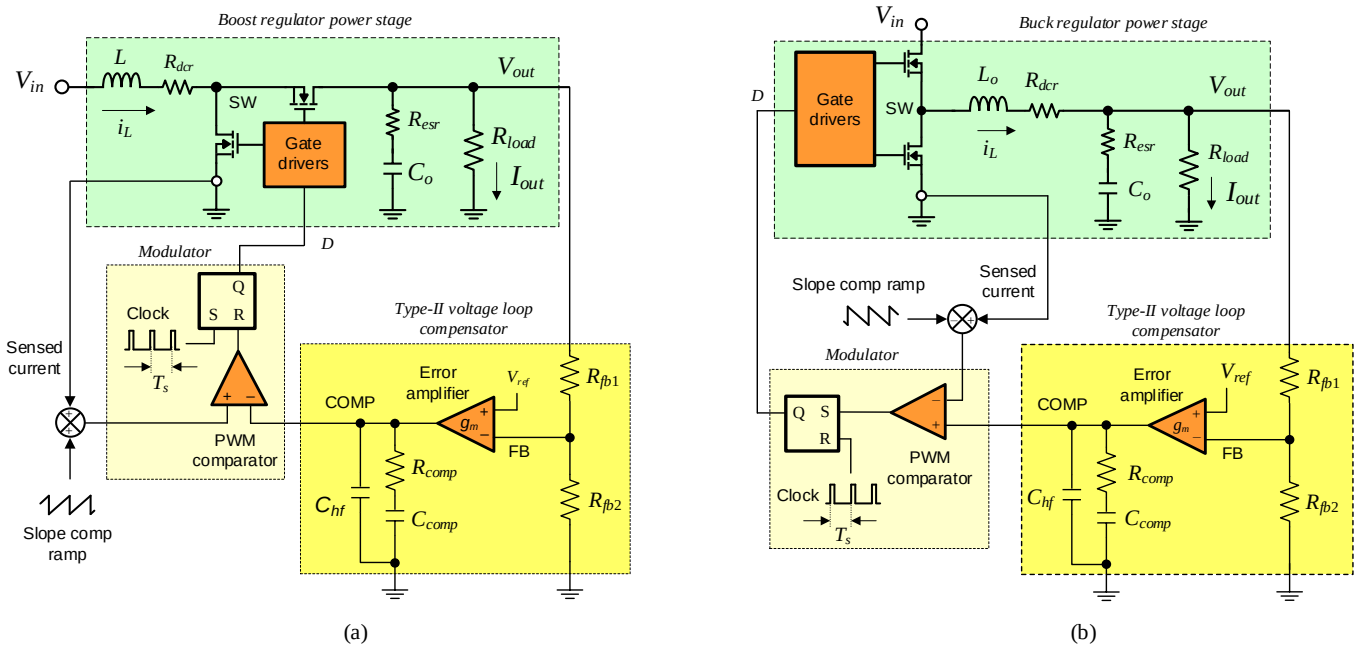


Fig. 1. Dc-dc regulator circuit schematics of the power stage and control-loop structure for peak current-mode boost (a) and valley current-mode buck (b).

In a peak or valley current-mode architecture, the state of the inductor current is naturally sampled by the PWM comparator. And while the typical circuit diagram of the loop architecture has seemingly few parts, the current-feedback loop is quite nonlinear, having discrete-time behavior. Meanwhile, the outer voltage loop employs a conventional type-II compensation circuit, shown in Fig. 1 with a transconductance error amplifier (EA) with its inverting input, labeled as the feedback (FB) node and connected to feedback divider resistors designated R_{fb1} and R_{fb2}. The logic state of the PWM latch output in Fig. 1 is suitably assigned for the particular peak or valley implementation (with trailing- or leading-edge modulation, respectively).

A compensated error signal appears at the EA output, designated as COMP, with the outer voltage loop giving the reference command for the inner current loop. The COMP voltage effectively represents the programmed inductor current level. The current loop converts the inductor into a quasi-ideal voltage-controlled current source: a means by which the inductor is removed from the outer loop dynamics, at least at dc and low frequencies.

Current Sensing And Subharmonic Oscillation

The current-sense (CS) implementation can be a shunt resistor placed in series with the inductor or one of the switches, or lossless current sensing using switch on-state resistance or inductor DCR. Likewise, integrating the switches and controller using a monolithic die (or copackaged as a multichip module) facilitates lossless current sensing. In any case, equation 1 gives the amplifying multiple for CS gain as:

$$R_i = G_i R_s \qquad (1)$$

where G_i is the gain of the CS amplifier and R_s is the current sensor gain. Furthermore, the amplified current signal is often level shifted such that the PWM comparator inputs are suitably biased over the full operating ranges of load current and input voltage.

A perfect current mode-controlled regulator relates only to the dc or average value of the inductor current. In practice, an error exists between the sampled current and the average inductor current. This error manifests as subharmonic oscillation at half the switching frequency with duty cycles greater or less than 50% for peak and valley operation, respectively. As I'll discuss later, subharmonic behavior is an issue with the current loop and can appear whether the voltage regulation loop is open or closed.

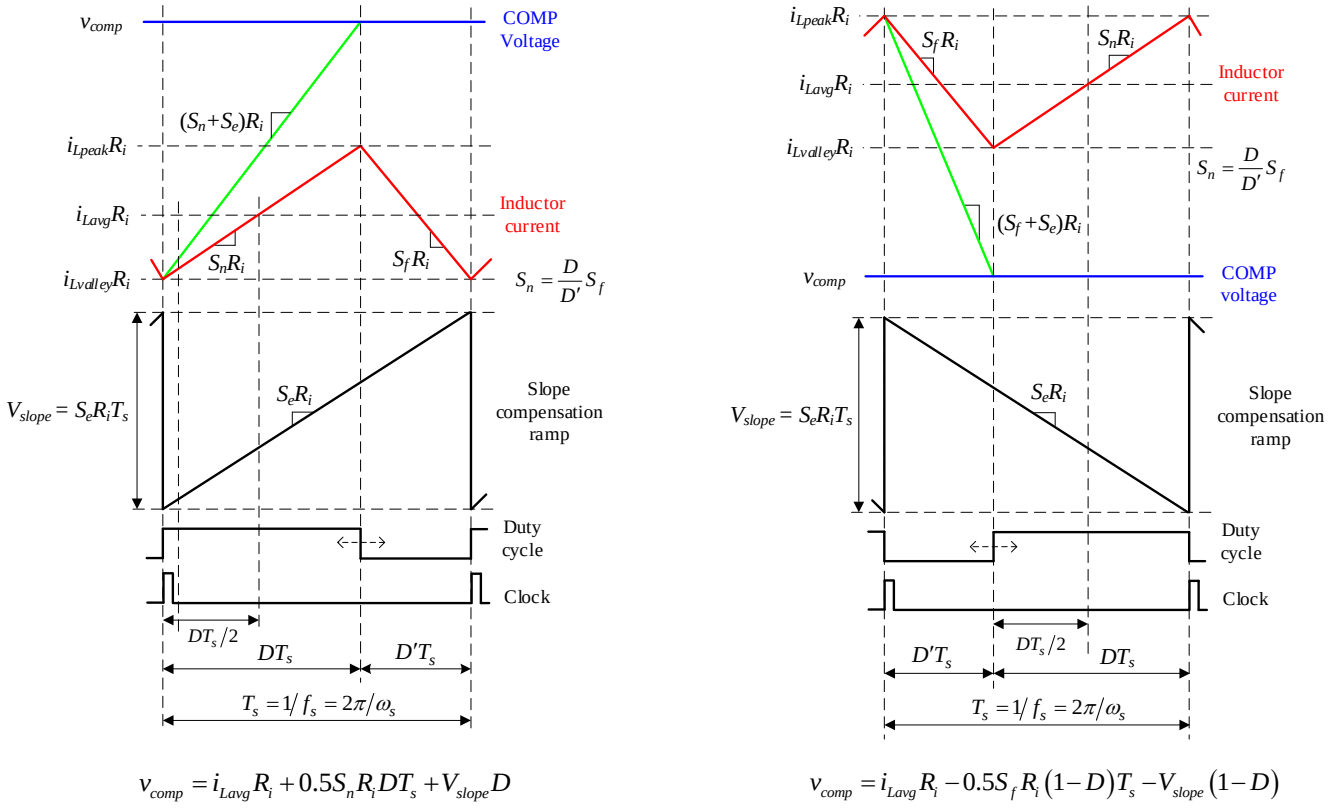
Current-Mode Operating Waveforms

Fig. 2a illustrates the waveforms for PCMC, and how a turn-on command for the control switch activates when the clock edge sets the PWM latch. The inductor current increases during the on-time, and a turn-off command occurs when the sensed inductor current peak plus the slope compensation ramp reaches the COMP voltage level. The PWM comparator resets the PWM latch, and the duty-cycle command is sent to the gate driver.

Correspondingly, Fig. 2b shows the same waveforms for VCMC. Here, a turnoff command is issued based on the clock edge, and turn-on occurs when the sensed inductor current valley minus the slope compensation ramp reaches the COMP voltage.

S_e in Fig. 2 designates the slope of the external compensation ramp, and S_n and S_f are the respective on-time and off-time slopes of the inductor current. These slopes are in units of amperes per second, and scaling by R_i gives the voltage slopes in units of volts per second internal to the controller. Figs. 2a and 2b represent trailing-edge and leading-edge modulation, respectively, based on whether the falling or rising edge of the control-switch drive signal is modulated.

As an interesting example where peak and valley architectures combine in one implementation, consider the four-switch noninverting buck-boost power stage[7] shown in Fig. 3. The circuit functions by using PCMC and VCMC for boost and buck operation, respectively, and conveniently uses the same low-side current-sensing element for both. During the buck-boost transition region when V_{in} is close or equal to V_{out}, the loop toggles between PCMC and VCMC by interleaving buck and boost switching pulses to support output voltage regulation.



$$v_{comp} = i_{Lavg}R_i + 0.5S_nR_iDT_s + V_{slope}D$$

(a)

$$v_{comp} = i_{Lavg}R_i - 0.5S_fR_i(1-D)T_s - V_{slope}(1-D)$$

(b)

Fig. 2. PWM waveforms for PCMC with trailing-edge modulation (a) and VCMC with leading-edge modulation (b).

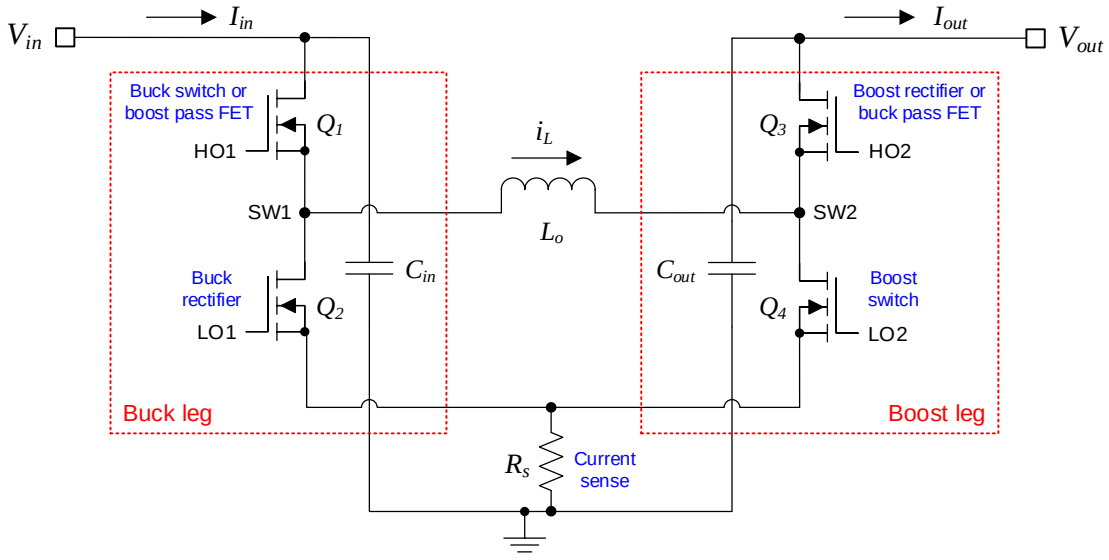


Fig. 3. Three operating modes for a four-switch buck-boost based on the input and output voltages: buck (V_{in} > V_{out}) with VCMC, boost (V_{in} < V_{out}) with PCMC, and buck-boost transition (V_{in} ≈ V_{out}) with a combination of PCMC and VCMC.

The Inner Current Loop

It's useful to understand the control-to-inductor current transfer function, otherwise stated as the gain linking the control voltage v_{comp} (the stimulus) to the inductor current i_L (the response). In this case, the regulator operates in open-loop conditions for output voltage regulation but works in closed loop for the inductor current.

Fig. 4 shows the inductor current representation following a perturbation, indicating a sampled system. The COMP voltage sets a dc command for the peak inductor current. The slope compensation ramp subtracts from the COMP voltage, equivalent to the previous method of adding a ramp to the CS signal—the method adopted in most commercial PCMC IC implementations (both options lead to the same peak current setpoint, of course).

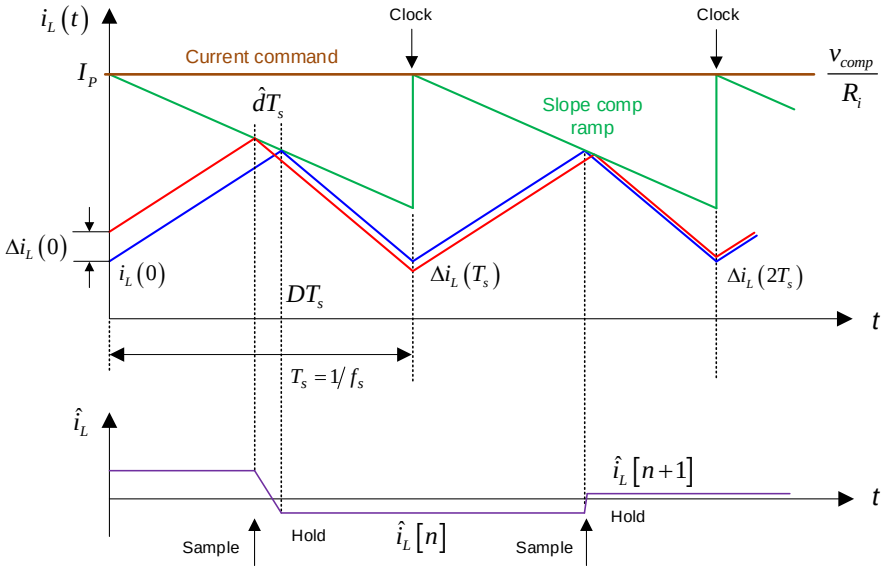


Fig. 4. The representation of an inductor current perturbation is that of a sample-and-hold system.

Christophe Basso offers an interesting treatment in reference 8 of the dynamics of the current loop cell, including analysis and simulation to highlight the underlying relationships between the current-loop response, slope compensation and loop stability. Building on Ray Ridley's seminal paper and Ph.D. thesis on peak current-mode control,[9-11] Basso imparts an intuitive derivation for the sampled-data expression in PCMC as

$$G_{vi}(z) = \frac{\hat{i}_L(z)}{\hat{v}_{comp}(z)} = \frac{1}{R_i}(1+\alpha)\cdot\frac{z}{z+\alpha} \qquad (2)$$

$$\text{where} \quad \alpha = \frac{S_f - S_e}{S_n + S_e}$$

The expression in equation 2 describes the sampling of the inductor current when its value meets the voltage command setpoint and the hold of the acquired value until the next sampling instant, depicted in Fig. 4. The pole located at $z_p = -\alpha$ must remain inside the unit circle to ensure stability, $|\alpha| < 1$. For instance, if S_e = 0, the condition for stability reduces to $S_n < S_f$, corresponding to $D < 0.5$ as expected.

Of course, the discretization in the z-domain is not conducive to study the current loop or to understand its frequency response. Fortunately, it is straightforward to convert equation 2 into the sampled Laplace domain by replacing z with e^{sT_s} and then into the continuous Laplace domain by supplementing with the transfer function of a zero-order hold given by equation 3:

$$H_{ZOH}(s)=\frac{1-e^{-sT_s}}{sT_s} \tag{3}$$

Combining equations 2 and 3 yields a reconstruction of a continuous-time function from the sampled sequence as

$$G_{vi}(s)=\frac{\hat{i}_L(s)}{\hat{v}_{comp}(s)}=\frac{1}{R_i}(1+\alpha)\frac{e^{sT_s}}{e^{sT_s}+\alpha}\frac{1-e^{-sT_s}}{sT_s}=\frac{1+\alpha}{R_i}\frac{1}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha} \tag{4}$$

Referring to Ridley's work, the model of the current-mode converter designates a block $H_e(s)$ to describe the sampling effects of the current loop. Ridley placed this block after sense resistor R_i in the current-loop feedback path, in contrast to the forward path after the modulator as proposed by other researchers.

Now pursuing the transfer function for $H_e(s)$, Fig. 5 shows a block diagram model highlighting the inner current loop with the COMP voltage as the sole stimulus. The input and output voltages are effectively ac-zeroed.[8]

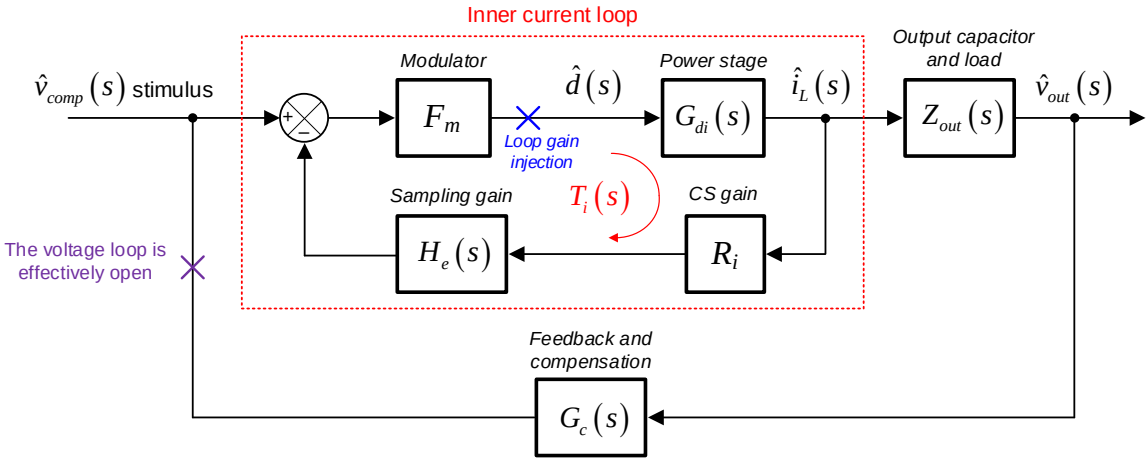


Fig. 5. Block diagram showing the inner current loop.

Equation 5 describes the COMP voltage-to-inductor current transfer function based on Fig. 5 as

$$G_{vi}(s)=\left.\frac{\hat{i}_L(s)}{\hat{v}_{comp}(s)}\right|_{\hat{v}_{in}(s)=0}=\frac{F_m G_{di}(s)}{1+F_m G_{di}(s)H_e(s)R_i} \tag{5}$$

where F_m and $G_{di}(s)$ designate the modulator gain and duty-cycle-to-inductor current continuous-time transfer function, respectively.

From Fig. 2, equation 6 expresses the small-signal gain of the modulator, with the clock initiating the on-time akin to that for voltage-mode control:[9-10, 12]

$$F_m=\frac{\hat{d}(s)}{\hat{v}_c(s)}=\frac{1}{(S_n+S_e)R_iT_s}=\frac{1}{m_cS_nR_iT_s} \tag{6}$$

where the slope compensation parameter is $m_c=1+S_e/S_n$.

If the COMP voltage remains constant, the modulating source driving the impedance is $d(s)V_{in}$ and the duty cycle-to-inductor current transfer function for a buck power stage is

$$G_{di}(s)=\frac{\hat{i}_L(s)}{\hat{d}(s)}=\frac{V_{\text{in}}}{Z_L(s)+Z_{out}(s)}=\frac{V_{\text{in}}}{sL_o+R_{dc}+\left(R_{esr}+\frac{1}{sC_o}\right)\|R_{load}} \tag{7}$$

Neglecting resistive parasitics gives

$$G_{di}(s)=\frac{V_{in}(1+sR_{load}C_o)}{R_{load}+sL_o(1+sR_{load}C_o)}\approx\frac{V_{in}}{sL_o}=\frac{1}{R_i}\frac{S_n+S_f}{s} \tag{8}$$

Equating equations 4 and 5 and substituting equations 6 and 8 then yields

$$\frac{F_mG_{di}(s)}{1+F_mG_{di}(s)R_iH_e(s)}=\frac{1+\alpha}{R_i}\frac{1}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha} \tag{9}$$

And the sampling gain thus results in

$$H_e(s)=\frac{sT_s}{e^{sT_s}-1} \tag{10}$$

Simplifying $H_e(s)$ using a second-order Padé approximation gives a simple polynomial expression describing a pair of right-half-plane (RHP) zeroes located at half the switching frequency (and contributing a 90° phase lag at that frequency), as follows:

$$H_e(s)\approx 1-\frac{s}{\omega_s/\pi}+\left(\frac{s}{\omega_s/2}\right)^2=1+\frac{s}{Q_z\omega_n}+\left(\frac{s}{\omega_n}\right)^2$$
$$\text{where}\quad Q_z=\frac{-2}{\pi},\quad \omega_n=\frac{\omega_s}{2}=\frac{\pi}{T_s} \tag{11}$$

Fig. 5 shows an equivalent circuit to determine the loop gain of the inner current loop, designated as $T_i(s)$ and measured by breaking the loop at the output of the duty-cycle modulator. Using equations 6 and 8 gives

$$T_i(s)=F_mG_{di}(s)H_e(s)R_i=\frac{1}{m_cS_nR_iT_s}\frac{V_{in}(1+sR_{load}C_o)}{R_{load}+sL_o(1+sR_{load}C_o)}H_e(s)R_i \tag{12}$$

With $S_n=V_{in}D'/L_o$, there is a low-entropy form that aligns with Ridley's derivation in his thesis,[10] expressed as

$$T_i(s)=\frac{L_o}{R_{load}T_sm_cD'}\frac{1+sR_{load}C_o}{\Delta(s)}H_e(s) \tag{13}$$

and the double pole associated with the output filter of the power stage is

$$\Delta(s) = 1 + \frac{s}{Q_{ps}\omega_o} + \left(\frac{s}{\omega_o}\right)^2$$

$$\text{where} \quad Q_{ps} = \frac{1}{\omega_o\left(\frac{L_o}{R_{load}} + R_{esr}C_o\right)}, \qquad \omega_o = \frac{1}{\sqrt{L_o C_o}} \tag{14}$$

Basso describes how subharmonics oscillation finds its underpinnings in the gain of the current loop when its crossover frequency is set too high. Note that the slope compensation parameter m_c inversely affects the dc gain but does not impact the pole and zero locations (and thus the phase). As shown in Fig. 6 using a typical design with TI's LM5137F-Q1[4] buck controller, increasing the compensation ramp lowers the whole current-loop gain curve and sets the crossover where the phase margin favorably improves.

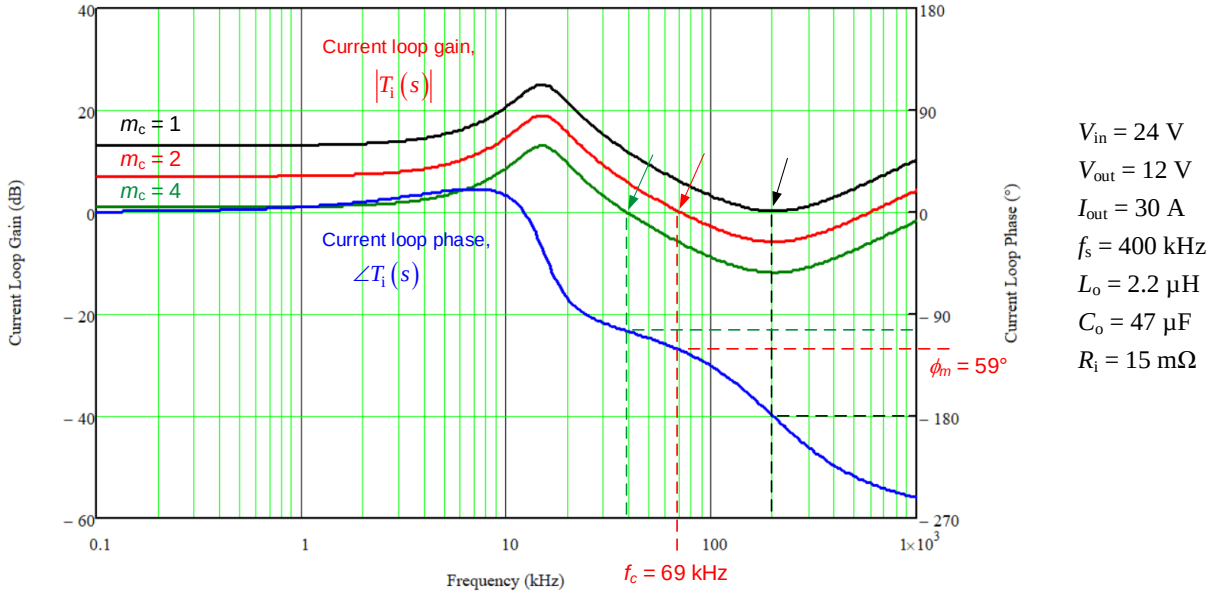


Fig. 6. Bode plots of the current loop in a CCM buck regulator showing the low-frequency zero, complex double poles and $H_e(s)$ complex RHP zeros.

Fig. 6 directs that a high current-loop crossover giving a low phase margin is the root cause of subharmonic oscillations. By setting a 100% compensation ramp (S_e = S_n, m_c = 2) in this example, the crossover frequency and phase margin of the current loop are 69 kHz and 59°, respectively.

The Outer Voltage Loop

Suitable for deriving the control-to-output transfer function, Fig. 7 shows the block diagram model from Fig. 5 with the outer voltage regulation loop closed. $G_c(s)$ defines the compensator transfer function that includes the feedback resistor-divider network.

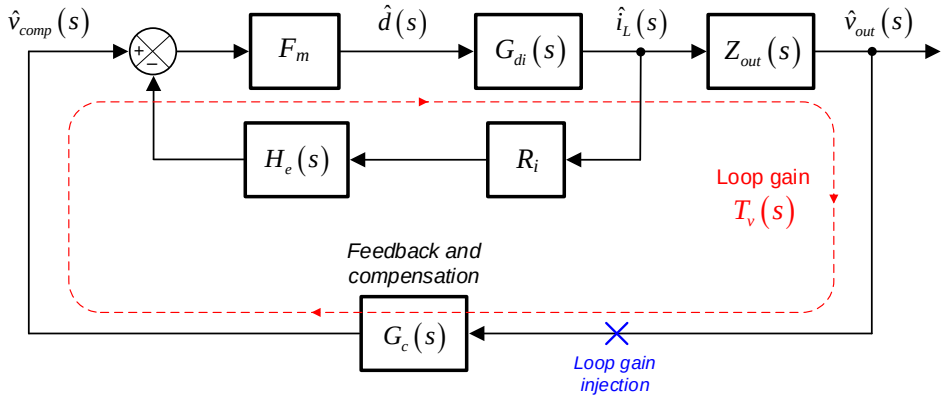


Fig. 7. Simplified control-loop block diagram. As before, $H_e(s)$ is the sampling gain placed in the current-loop feedback path.

Various treatments exist in the literature to derive the loop gain; see Feucht[12] and Sheehan.[13-14] Still widely appreciated is Ridley's approach, shown in Fig. 8, for the full model of a buck regulator using the PWM switch model.

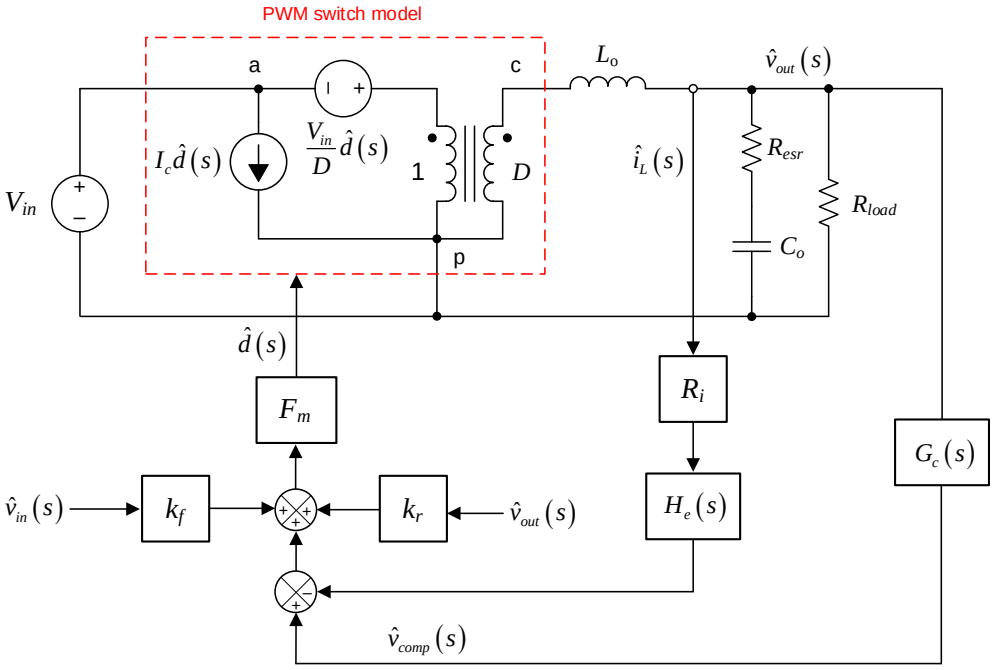


Fig. 8. Loop gain using a buck regulator model with a closed current loop.

With the input voltage perturbation set to zero, Ridley derives the control-to-output transfer function in pole/zero form as equation 15:

$$G_{c\text{-}o}(s) = \frac{\hat{v}_{out}(s)}{\hat{v}_{comp}(s)}\bigg|_{\tilde{v}_{in}(s)=0} = A_{dc}\frac{1+\dfrac{s}{\omega_{esr}}}{1+\dfrac{s}{\omega_p}}H(s) \qquad (15)$$

The dc gain coefficient and frequencies for the dominant (load) pole and capacitor ESR zero are

$$A_{dc} = \frac{R_{load}}{R_i}\frac{1}{k_d} \tag{16}$$

$$\omega_p = 2\pi f_p = \frac{k_d}{R_{load}C_o} \tag{17}$$

$$\omega_{esr} = 2\pi f_{esr} = \frac{1}{R_{esr}C_o} \tag{18}$$

where

$$k_d = 1 + \frac{R_{load}T_s}{L_o}\left(m_c D' - 0.5\right) \tag{19}$$

H(s), the high-frequency extension in the control-to-output transfer function designed to model the modulator sampling gain, is a pair of complex poles at a half switching frequency, given by

$$H(s) = \frac{1}{1 + \frac{s}{Q\omega_n} + \frac{s^2}{\omega_n^2}} \tag{20}$$

Equation 21 defines the quality factor:

$$Q = \frac{1}{\pi\left(k - 0.5\right)}, \quad k = m_c D' \tag{21}$$

The RHP zero pair, located at half switching frequency in the current-loop gain, actually becomes subharmonic poles in the control-to-output transfer function once the outer voltage loop closes. The compensation ramp naturally dampens these subharmonic poles.

For single-cycle damping of an inductor-c perturbation in a PCMC buck regulator, the slope compensation ramp should equal the inductor current downslope. This is also evident graphically from Fig. 4, where a perturbed inductor current will revert to its original value in one switching cycle. The resultant fixed value of *Q* is 0.637, calculated by

$$\begin{aligned} S_e = S_f &= \frac{D}{D'}S_n = \frac{V_{out}}{L_o}R_i \\ m_c &= 1 + \frac{S_e}{S_n} = 1 + \frac{D}{D'} = \frac{1}{D'} \\ k &= m_c D' = 1 \\ Q &= \frac{1}{\pi\left(k - 0.5\right)} = \frac{2}{\pi} = 0.637 \end{aligned} \tag{22}$$

From equation 13, repeated here,

$$T_i(s) = \frac{L_o}{R_{load} T_s m_c D'} \frac{1 + sR_{load} C_o}{\Delta(s)} H_e(s)$$

you can see that the current-loop gain does not vary with input voltage if $m_c = 1/D'$. Note that excessive slope compensation increases m_c, decreases Q, and reduces the current-loop gain and crossover. This implies additional phase lag in the voltage loop and restricts the maximum attainable crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts toward voltage-mode control.

Conversely, insufficient slope compensation decreases m_c and increases Q, causing poor phase margin in the current-loop gain and ultimately voltage-loop instability as the duty cycle approaches or exceeds 50%. Having a Q value in the range of 0.5 to 1.0 is generally satisfactory.

Based on the design used for Fig. 6 and with m_c = 2, Fig. 9 provides a control-to-output frequency response, with × and o symbols denoting the respective pole and zero locations. The transfer function shows a three-pole system, comprising the dominant load pole and the double pole at a half switching frequency related to the sampling gain.

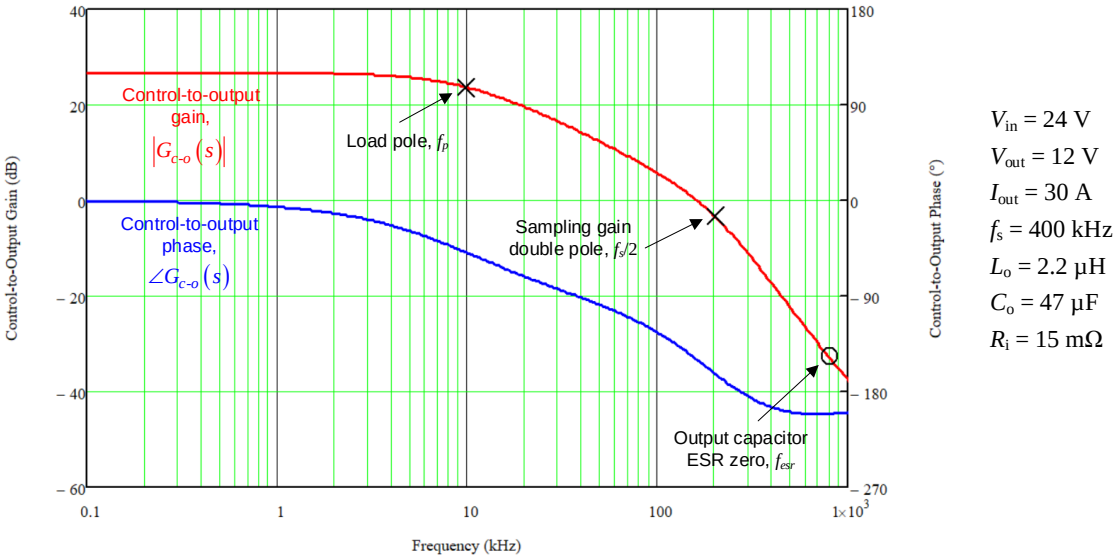


Fig. 9. Control-to-output response of a typical buck regulator.

Summary

A primary objective of this article is to provide an overview of the small-signal behavior of a current mode-controlled dc-dc regulator, which is important to understand for any designer looking to apply current-mode control. This article reviews the specific attributes pertaining to peak and valley current-mode architectures and examines the inner current loop gain and its impact on the control-to-output transfer function.

Although engineers will typically not measure the frequency response of the inner current loop when designing a current mode-controlled regulator, it is useful to understand the phenomenon at play with regard to slope compensation. Part 2 of this article series will discuss loop-compensation design for practical current-mode circuits.

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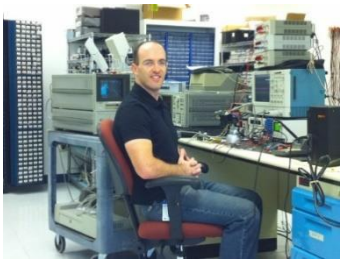
About The Author



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For further reading on current mode control, see the "How2Power Design Guide," locate the Design Area category and select Control Methods.