ISSUE: December 2024

Designing An Open-Source Power Inverter (Part 22): Converter Regulator Dynamics

by Dennis Feucht, Innovatia Laboratories, Cayo, Belize

Having addressed the magnetics and control circuit design in recent parts of this series[1-21], we now address other elements of designing the Volksinverter's battery converter stage (Fig. 1). These relate to regulator dynamics affecting the response of the converter.

The converter voltage regulator loop traverses BCV401 and BCV402 Volksinverter modules. The output storage capacitor C_o is yet to be determined along with the BCV402 current-sense amplifier within the larger voltage control loop that includes some of the BCV401 circuitry. Design aspects of these circuits are expounded here. That extends to a derivation of the transfer functions for the voltage control loop of the battery converter based on our choice of the CA (boost) converter topology.

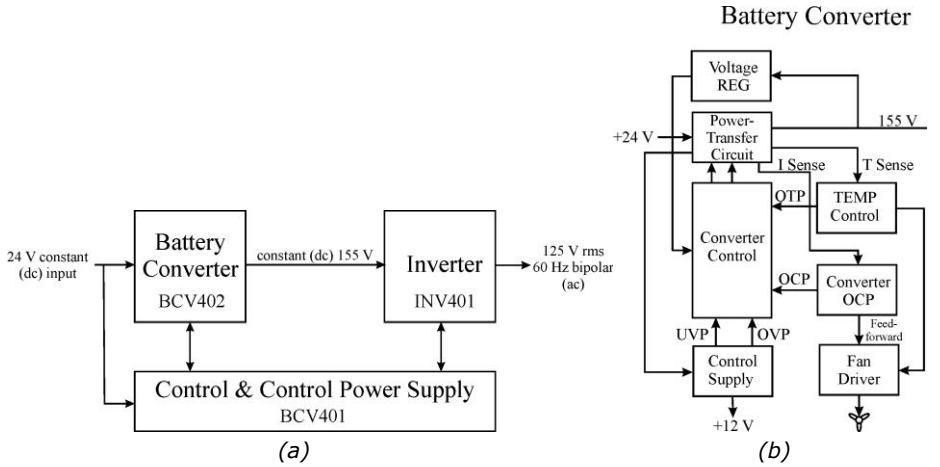

Fig. 1. The Volksinverter's system block diagram (a) and the BCV402 battery converter stage block diagram (b). This part of the series addresses selection of the output storage capacitor and current-sense circuitry residing on BCV402 (see Fig. 2) as well as the voltage control loop error amplifier which is on BCV401 (see Fig. 3). Transfer functions for the voltage control loop are also derived.

Storage Capacitor Sizing

The Volksinverter BCV402 power-transfer circuit shown in Fig. 1 has output storage capacitor C_o (C2). It averages the output voltage Vc (VC+) to keep it nearly constant and present a voltage source to the inverter-stage input. To the inverter stage, C_o supplies current during boost (CA) switch-cycle on-time.

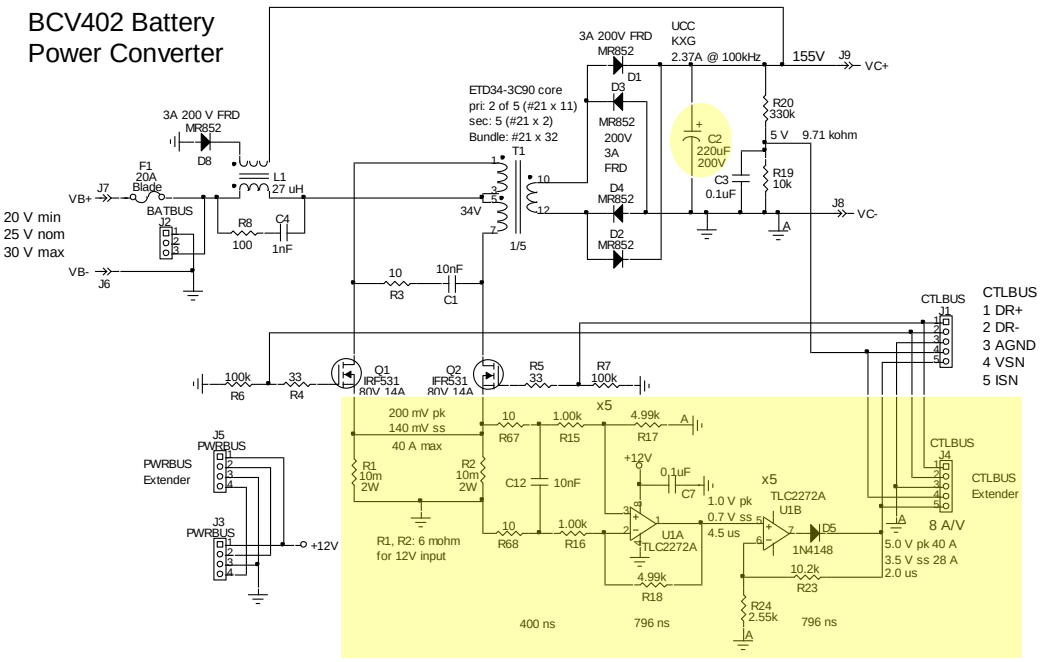

Fig. 2. BCV402 boost push-pull battery converter power-transfer circuit, including transformer magnetics design notes. The output storage capacitor C_o = C2 and current sense amplifier are highlighted here. Current-sense scaling allows for higher-current MOSFETs than Q1 and Q2 with reduction of sense-resistance R1 and R2 values.

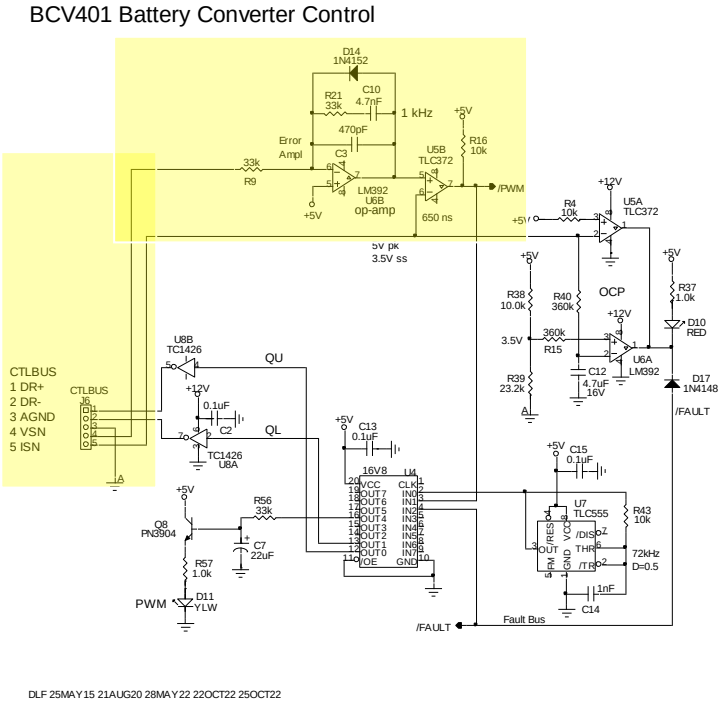

Fig. 3. BVC401 control subsystem for the battery converter stage. The error amplifier circuitry for the voltage control loop is highlighted here. (This schematic diagram originally appeared as Fig. 4 in part 19.[19])

Ideally, C_o is infinite and thus is an ideal voltage source. Electrolytic capacitors approach the ideal in practice because they have large capacitance with low series resistance. What is the right value for C_o? The Volksinverter output waveform is a "third-harmonic sine-wave" (3HSW), as developed in part 4[4] and shown here in Fig. 4. It has output *crest factor* χ_o and *form factor* κ_o;

$$\chi_o = \frac{\hat{i}}{\tilde{i}} = 1.223 \; ; \; \kappa_o = \frac{\tilde{i}}{\bar{i}} = 1.073 \Rightarrow \frac{\hat{i}}{\bar{i}} = \chi_o \cdot \kappa_o = 1.313$$

Where superscript ~ denotes rms, ^ denotes peak, and – denotes average. The optimal relative amplitude of the third-harmonic sine-wave was derived in part 4[4] with these waveform characteristics.

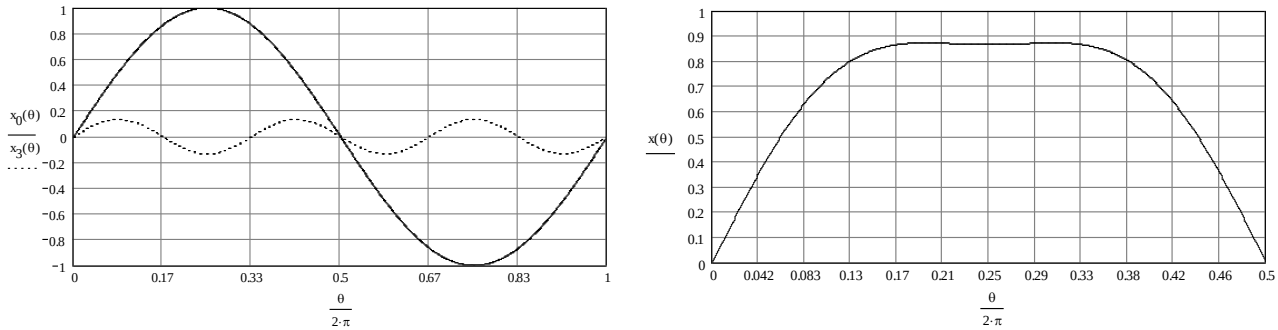

Fig. 4. Fundamental and third-harmonic sine-waves (left), combined in optimal proportions into a third-harmonic sine-wave (3HSW). The 3HSW positive half-cycle is shown (right).

Output power is scaled by design to $\bar{P}_o$ = 333 W at an average C_o voltage of V_c = 160 V. Capacitor C_o voltage v_C varies because of its ripple component and is the peak voltage of the inverter output waveform. Average converter output current is $\bar{i}_O = \bar{P}_o / V_c$ = 2.08 A. If the voltage control loop of the converter is not fast enough to maintain a constant V_c (from a quick load change), then the rectifier ripple current amplitude supplied to C_o is

$$\hat{i}_{C\sim} = \hat{i}_O - \bar{i}_O = \bar{i}_O \cdot \left(\frac{\hat{i}_O}{\bar{i}_O} - 1 \right) = (2.08\,\text{A}) \cdot (1.313 - 1) = 0.651\,\text{A}$$

The average capacitor current in steady-state must of course be zero. Thus $\hat{i}_{C\sim}$ is the half-cycle average of capacitor ripple current. It corresponds to calculations based on the 3HSW half-cycle of Fig. 4 (right).

From the Fig. 4 graph (right), the 3HSW peak extends longer in time than the sine wave (of the left graph) and charges C_o longer and at a lower current. The form factor of i_C is lower and thus RMS current $\tilde{i}_C$ is lower, reducing ohmic loss in C_o. The duration of the peak is about from the horizontal-axis value of 0.17 to 0.34. The C_o discharge time is symmetric on each side of this peak, with a duration of $\Delta\theta/2\cdot\pi$ = 0.17 + (0.5 – 0.34) = 2·(0.17) = 0.34 of the 3HSW cycle. Then the discharge time is

$$\Delta t = (0.34)\cdot(T_g/2) = (0.34)\cdot(1/120\text{ Hz}) = 2.833\text{ ms}$$

C_o voltage ripple is twice its ripple amplitude, or

$$\Delta v_C = 2 \cdot \hat{v}_{C\sim} = 2 \cdot \frac{(0.651\,\text{A}) \cdot (2.83\,\text{ms})}{C_o} = \frac{3.685\,\text{mC}}{C_o}$$

A 1-mF capacitor has ripple voltage Δv_C = 3.685 V. At a nominal 160-V output, valley and peak voltages of v_C are

$$\breve{v}_C \approx 158 \text{ V} \; ; \; \hat{v}_C \approx 162 \text{ V} \; , \; V_c = 160 \text{ V}$$

The control loop of the BCV401 and BCV402, scaled for $\bar{P}_o$ = 333 W, holds v_C constant at an average of $v_O = V_c$ and at full-scale operation, for Δv_C = 3.685 V, the required C_o is

$$C_o = \frac{(\hat{i}_C - \bar{i}_C)\cdot\Delta t}{\Delta v_C} = \frac{\Delta t}{\Delta v_C}\cdot\left(\frac{\hat{i}_C}{\bar{i}_C} - 1\right)\cdot\bar{i}_C = \frac{2.833\,\text{ms}}{3.685\,\text{V}}\cdot(0.313)\cdot\bar{i}_C = (240.6\,\mu\text{F/A})\cdot\left(\frac{\bar{P}_o}{V_c}\right) \Rightarrow$$

$$\frac{C_o}{\bar{P}_o} = \frac{240.6\,\mu\text{F/A}}{160\,\text{V}} = 1.504\ \mu\text{F/W} = 1504\ \mu\text{F/kW}$$

For a converter of 333 W, C_o = (1504 µF/kW)·(0.333 kW) = 501 µF. Ripple will be greater when capacitor series resistance is included. At 220 µF for C2, a single BCV402 has ripple voltage of about Δ8.4 V = ±4.2. A single BCV402 with 470 µF will fit the same board pattern and is the nearest commercial value.

Another limit on how small C_o can be made is capacitor current rating. A Nichicon 220-µF, 200-V Al electrolytic capacitor is rated for a maximum current of 1.88 A. At an fs output current of $\bar{i}_O$ = 2.08 A, this rating is exceeded somewhat and a larger capacitor of at least 470-µF is required to provide an adequate reliability margin for C_o. Thus, C2 = 220 µF is pushing the current rating for a Nichicon capacitor, one of the best in the industry.

Current-Sense Amplifier

The BCV402 current-sense circuit is shown in Fig. 5, a three-stage amplifier with a 1.2-µs risetime. The first stage is a passive RC integrator that attenuates the high frequencies of fast current "glitches" at switching times, especially when switching on. The time-constant is comparable to the switch time.

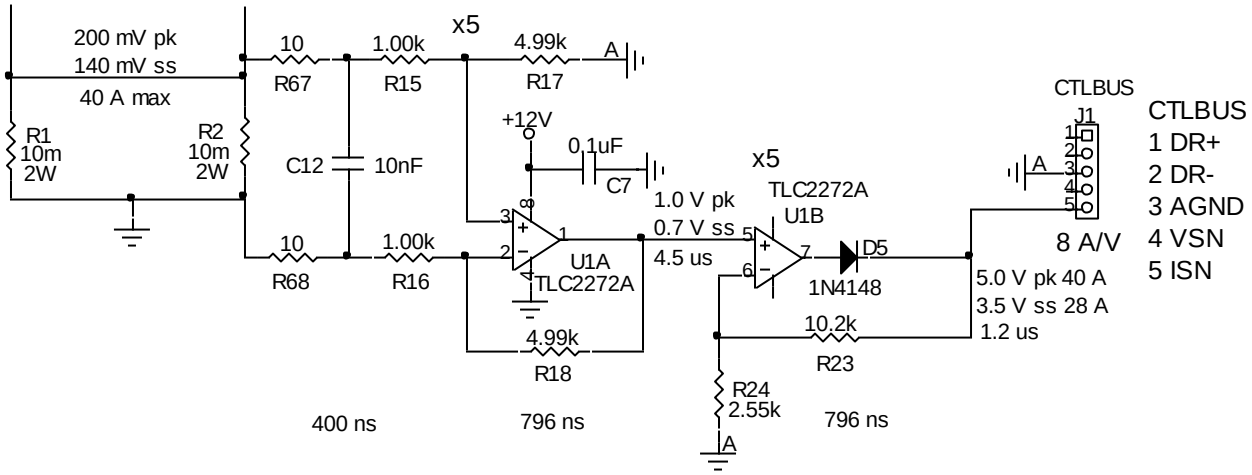

Fig. 5. The BCV402 current-sense amplifier consisting of two active stages, U1A and U1B. Both stages have a gain of ×5, or ×25 total, resulting in a scale factor of 8 A/V for 5 mΩ of sense resistance. The TLC2272A has a unity-gain frequency f_T = 2.2 MHz. The first stage differential RC integrator has a risetime of 400 ns. Total risetime is 1.2 µs.

The U1A and U1B op-amp stages each have a closed-loop gain of 5. The first stage is a one-op-amp diff-amp and the second is noninverting and ground-referenced. The TI TLC2272A dual op-amp has a unity-gain

frequency f_T = 2.2 MHz. The closed-loop bandwidth at a gain of 5, given a single-pole (–1 slope) roll-off of the op-amp open-loop gain, is

$$f_{bw} = 2.2 \text{ MHz}/5 = 440 \text{ kHz}$$

The current-sense amplifier drives the PWM comparator U5B of the BCV401, shown in Fig. 6. It drives logic which drives gate drivers and the power switches. Combined, this *control delay time* t_{cd} is the time required for power circuits to protect themselves; t_{cd} is as fast as the active loop can respond. Previously, t_{cd} was given as 2 µs. The comparator responds in about 450 ns (at high di/dt), the logic and gate drivers in 50 ns, and MOSFETs shut off in about 300 ns giving a combined 2-µs allotment for t_{cd}.

The grounds marked "A" in Fig. 3 are "analog grounds", 0-V nodes that are connected separately to the ground source from the supply to avoid noise as extraneous voltage drops across their traces from power-circuit currents. They are an elaborate way of implementing four-wire sensing of current, with separate drive and sense connections at the source.

The R1 and R2 sense resistors themselves are given similar attention in board layout interconnection. Finally, diode D5 of amplifier U1B effects an analog wire-OR when multiple BCV402 current amplifier outputs are paralleled. This logic connection allows the highest voltage (and hence current) to prevail in feedback to the PWM comparator and is a max{i} function instead of a logic OR function.

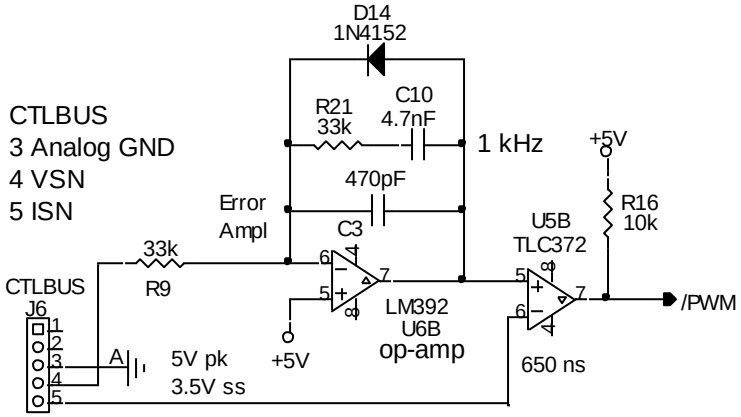

Fig. 6. BCV401 error amplifier U6B, part of the voltage control loop. VSN is the attenuated converter output voltage v_C and ISN is the amplified current-sense voltage, both from the BCV402 module.

Voltage Control Loop

Converter dynamic response to a small change in v_C—that is, incremental $v_C = v_c$—whether caused by C_o charge cycling each inverter half-cycle or by a transient load change, is characterized by the voltage control loop. If its response time is too slow, v_C can cause amplitude undervoltage or overvoltage of the inverter output waveform v_g. If it is too fast and approaches the bandwidth of the inner peak-current control loop, it could amplitude-modulate v_C. The block diagram of the entire converter model is shown in Fig. 7, where A_{Ce} = 1 and A_{Ve} is the voltage error amplifier.

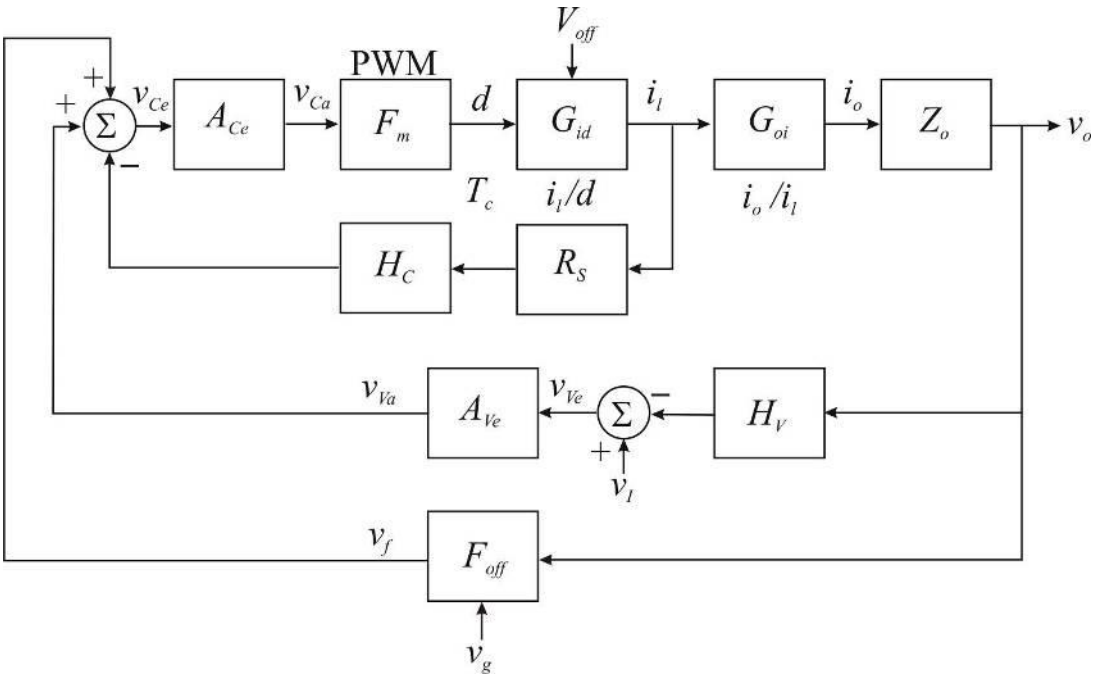

Fig. 7. Block diagram of the converter. Output $v_o = v_c$, H_V is the voltage divider R19, R20, A_{Ve} is the voltage-loop error amplifier U6B, U5B is F_m, R_S·H_C is the current-sense circuit of the BCV402, A_{Ce} = 1, and the power-transfer circuit is G_{id}·G_{oi} where Z_o is the inverter load. V_{off} and F_{off} account for changes in port voltages on dynamics.

The current loop has a switching frequency of $f_s >> f_g$, the inverter output frequency. The BCV401 voltage error amplifier A_{Ve} commands the peak current for the inner current-regulating loop as v_{Ce} (= v_{Ca}). If voltage-loop bandwidth $f_{bw} < f_g$ then the voltage loop will command a relatively constant input to the current loop of $\bar{i}_C$. The control circuit from Fig 6 is repeated here.

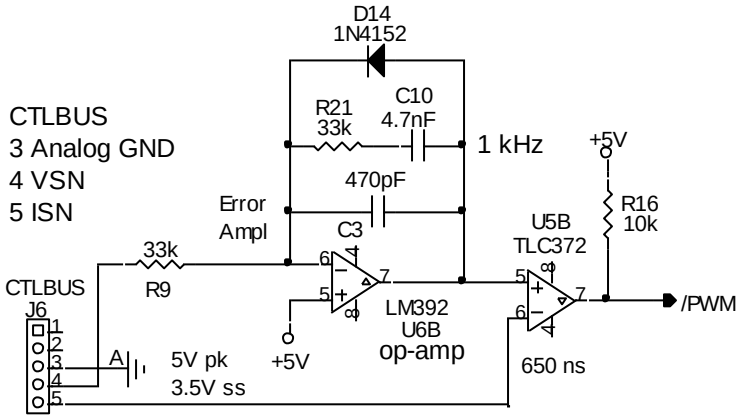

Fig. 6 again. BCV401 error amplifier U6B, part of the voltage control loop. VSN is the attenuated converter output voltage v_C and ISN is the amplified current-sense voltage, both from the BCV402 module.

The U6B error amplifier is an inverting op-amp that has two feedback branches. The series RC of R21 and C10 form a time-constant of a zero, τ_z = R21·C10 = 155 µs, corresponding to a frequency $f_z = 1/2{\cdot}\pi{\cdot}\tau_z \approx 1026$ Hz. The BCV402 divider R19 and R20 of Fig. 1 outputs $v_C/34$ behind a series resistance of 9.71 kΩ. Then op-amp

input resistance is R_i = R9 + 9.71 kΩ = 42.71 kΩ. C3 forms an RC integrator with R_i, forming a pole at the origin with a unity-gain time-constant of

$$\tau_{p0} = R_i \cdot (C10 + C34) = (42.71\ k\Omega) \cdot (5.17\ nF) = 221\ \mu s \Rightarrow f_{p0} = 721\ Hz$$

corresponding to frequency $f_{p0} = 1/2 \cdot \pi \cdot \tau_{p0}$ = 721 Hz. It causes amplifier gain to decrease at a −1 slope with frequency on a log-log plot (or −20 dB/dec, where 20 dB is a decade) to a gain magnitude of about 0.70 where the zero at f_z flattens the gain plot to a slope of zero.

A second error-amplifier pole is at time-constant

$$\tau_{pf} = R21 \cdot (C10 \parallel C3) = R21 \cdot [C10 \cdot C3/(C10 + C3)] = (33\ k\Omega) \cdot (427.3\ pF) = 14.1\ \mu s \Rightarrow f_{pf} = 11.29\ kHz$$

where || is *not* a topological descriptor but is defined as the math operator

$$x \parallel y = \frac{x \cdot y}{x + y}$$

For capacitances, it is the series-C formula. Thus, the error amplifier has a gain magnitude of about 0.7 above f_z, and with sign included is −0.7 as an inverting op-amp. The pole at f_{pf} is about a decade higher than f_z and has little effect on the dynamic response. (Poles and zeros separated by a decade have a phase contribution of about 6°.)

The frequency range of response of the voltage control loop above f_z extends to near f_{pf} and we can exclude the effect of the f_{pf} pole. Poles or zeros a decade or more above the loop gain-of-one or unity-gain frequency f_T have essentially no effect on feedback-loop behavior. (That is why it is not necessary to include in feedback analysis every high-frequency parasitic pole and zero in the circuit.)

The combined incremental gain from converter output v_c to error-amplifier output v_{Va} above f_z is about −0.70/34 = −1/48.6. Below f_z, the amplifier gain (magnitude) increases with decreasing frequency so that loop gain is large at low frequencies where the accuracy of the loop is required for steady-state operation. At $f_z/34 = f_{p0}/48.6$ = 21 Hz, the amplifier incremental gain magnitude $v_c/v_{Va} \approx 1$. The loop responds closer to the average voltage of the 60-Hz inverter waveform and the C_o formula in the previous section applies.

Also in the loop is the power-transfer circuit, a discontinuous nonlinear, discrete-time circuit that (quite happily) can be approximated as a linear incremental circuit. Design of the voltage control loop is an exercise in continuous (analog) circuit control. The Z_o load was previously considered involving C_o. F_{off} forms a feedback loop from the two power ports to include their voltage effects on circuit behavior.

We are assuming that previous inclusion of V_g and V_c ranges is adequate for design; that is, for dynamics we can hold the port voltages constant because they change much slower than switching waveforms. What remains is the incremental model of the power-transfer circuit. Although a more complete design involves considerable additional detail, to provide some insight into the equations for G_{id} and G_{oi} they are derived for the basic single-ended CA (boost) converter (excerpted from reference [22]).

CA (Boost) Converter Incremental Model

The CA (boost) converter steady-state transfer ratio is

$$\frac{V_o}{V_g} = \frac{I_g}{I_o} = \frac{1}{D'} \Rightarrow I_o = D' \cdot I_g \ ; \ V_g = D' \cdot V_o$$

The incremental *s*-domain circuit model is shown in Fig. 8. In the center of the diagram is the incremental model of the PWM-switch.

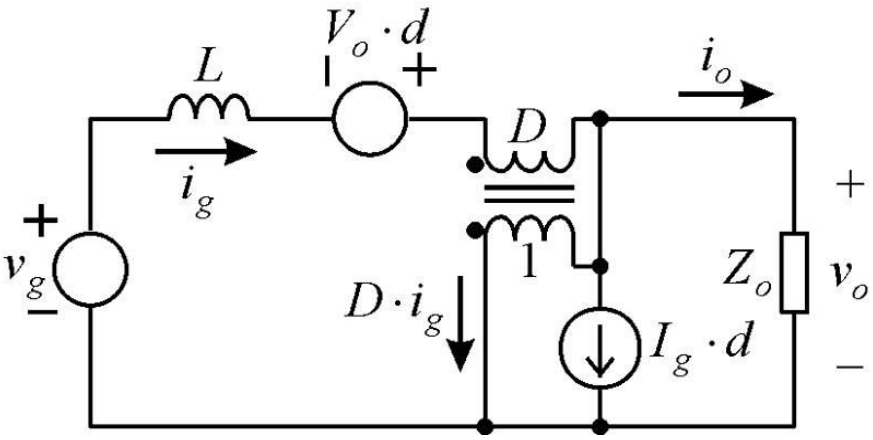

Fig. 8. Common-active PWM-switch converter linearized incremental circuit model. The circuitry in the center is the incremental SPDT PWM-switch model with active (on-time) conduction during duty-ratio D. D, I_g and V_o are the PWM-switch model parameters and are operating-point constants. Incremental variables are d, i_g and i_o.

The PWM-switch is a kind of active device, linearized by averaging its voltages and currents over a switch cycle. Linearized PWM-switch models for the three PWM-switch configurations are found in reference [22]. The CA (boost) steady-state output resistance R_o referred to the input port is

$$R_o' = \frac{V_g}{I_g} = \frac{D' \cdot V_o}{I_o / D'} = D'^2 \cdot R_o$$

R_o is "seen" at the input port as R_o'. The PWM-switch transforms R_o by D'^2 to appear at the input port as R_o'.

Applying the basic circuit laws of KCL, KVL and ΩL (Ohm's Law), the Fig. 6 circuit equations are

$$v_o = Z_o \cdot i_o$$
$$i_o = -I_g \cdot d - D \cdot i_g + i_g \Rightarrow i_o = -I_g \cdot d + D' \cdot i_g$$
$$s \cdot L \cdot i_g - V_o \cdot d - D \cdot v_o + v_o = 0\,\text{V} \Rightarrow s \cdot L \cdot i_g = V_o \cdot d - D' \cdot v_o$$

Substituting i_o from the first equation into the second equation,

$$i_o = \frac{v_o}{Z_o} = -I_g \cdot d + D' \cdot i_g \Rightarrow i_g = \frac{v_o}{D' \cdot Z_o} + \frac{I_g \cdot d}{D'} \Rightarrow v_o = Z_o \cdot (-I_g \cdot d + D' \cdot i_g)$$

Substituting for i_g in the third equation and solving,

$$s \cdot L \cdot \left(\frac{v_o}{D' \cdot Z_o} + \frac{I_g \cdot d}{D'} \right) = V_o \cdot d - D' \cdot v_o \Rightarrow$$
$$\frac{v_o}{d} = Z_o \cdot \frac{D' \cdot V_o - s \cdot L \cdot I_g}{s \cdot L + D'^2 \cdot Z_o} = \frac{V_o}{D'} \cdot \frac{s \cdot (-L'/R_o) + 1}{s \cdot (-L'/R_o) + 1}, \; L' = L/D'^2$$

where d is the incremental duty-ratio. The inductor referred through the PWM-switch to the output port is transformed to L'. The negative time-constant of the zero, $-L'/R_o$, is a right half-plane (RHP) zero and not helpful in producing stable loops. It is caused by the on-time delay of the CA circuit in delivering current to the output.

Next, substitute instead for v_o and solve;

$$s \cdot L \cdot i_g = V_o \cdot d - D' \cdot [Z_o \cdot (-I_g \cdot d + D' \cdot i_g)] \Rightarrow$$

$$\frac{i_g}{d} = \frac{i_l}{d} = \frac{V_o + D' \cdot I_g \cdot Z_o}{s \cdot L + D'^2 \cdot Z_o} = \left(\frac{V_o}{D'^2 \cdot Z_o} + \frac{I_g}{D'} \right) \cdot \frac{1}{s \cdot (L'/Z_o) + 1}$$

Substituting, $I_g/D' = V_o/D'^2 \cdot R_o$ and simplifying,

$$\frac{i_g}{d} = \frac{I_g}{D'} \cdot \frac{R_o + Z_o}{Z_o} \cdot \frac{1}{s \cdot (L'/Z_o) + 1}$$

The output capacitor C_o has series resistance R_c that contributes a significant zero within the voltage loop. Z_o is the load resistance R_o in parallel with the series RC of C_o and results in a zero at $R_c \cdot C_o$ and pole at $(R_c + R_o) \cdot C_o$;

$$Z_o = R_o \cdot \frac{s \cdot R_c \cdot C_o + 1}{s \cdot (R_c + R_o) \cdot C_o + 1}$$

Substituting Z_o,

$$\frac{v_o}{d} = \frac{V_o}{D'} \cdot \frac{(s \cdot R_c \cdot C_o + 1) \cdot (s \cdot (-L'/R_o) + 1)}{s^2 \cdot \left(L' \cdot C_o \cdot \frac{R_c + R_o}{R_o} \right) + s \cdot \left(\frac{L'}{R_o} + R_c \cdot C_o \right) + 1}$$

This is the transfer ratio of the final blocks in the voltage-control-loop forward path, $G_{id} \cdot G_{oi} \cdot Z_o$, from the PWM output to converter output $v_o = v_c$. The poles and zeros are plotted on the left-side graph of Fig. 9. The resonant frequency ω_n and damping ζ are

$$\omega_n = \frac{D'}{\sqrt{L \cdot C_o}} \cdot \sqrt{\frac{R_o}{R_c + R_o}} \approx \frac{1}{\sqrt{L' \cdot C_o}}, R_c << R_o, L' = L/D'^2$$

$$\zeta \approx \tfrac{1}{2} \cdot \left(\frac{Z_n'}{R_o} + \frac{R_c}{Z_n'} \right), \; Z_n' = \sqrt{L'/C_o}$$

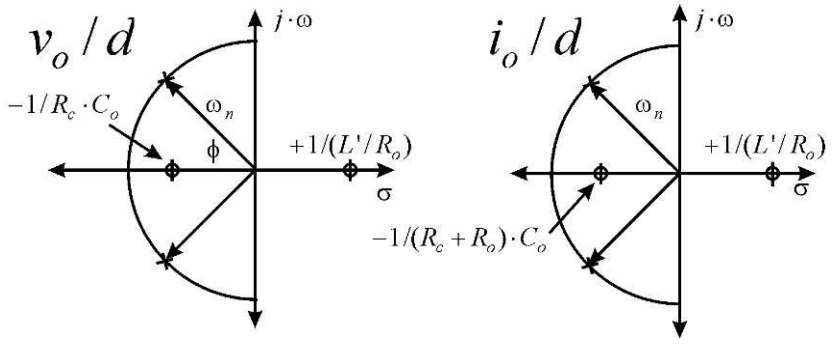

Fig. 9. Incremental transfer ratios from transfer-circuit duty-ratio input d to output voltage v_o or output current i_o, plotted in the s-domain as poles and zeros with complex pole angle (phase) ϕ and magnitude ω_n. The CA incremental output response has one complex pole-pair, a LHP zero and a RHP zero.

Continuing with CA transfer functions,

$$\frac{i_g}{d} = 2 \cdot \frac{I_g}{D'} \cdot \frac{s \cdot \frac{1}{2} \cdot [(2 \cdot R_c + R_o) \cdot C_o] + 1}{s^2 \cdot \left(L' \cdot C_o \cdot \frac{R_c + R_o}{R_o} \right) + s \cdot \left(\frac{L'}{R_o} + R_c \cdot C_o \right) + 1}$$

The next CA transfer function, graphed in Fig. 9, is

$$\frac{i_o}{d} = \frac{I_o}{D'} \cdot \frac{[-s \cdot L' / R_o + 1] \cdot [s \cdot (R_c + R_o) \cdot C_o + 1]}{s^2 \cdot \left(L' \cdot C_o \cdot \frac{R_c + R_o}{R_o} \right) + s \cdot \left(\frac{L'}{R_o} + R_c \cdot C_o \right) + 1}$$

All the transfer functions with *d* as input have the same pole-pair. The last CA transfer function is

$$\frac{i_o}{i_g} = \frac{i_o / d}{i_g / d} = \frac{1}{2 \cdot D'} \cdot \frac{[-s \cdot L' / R_o + 1] \cdot [s \cdot (R_c + R_o) \cdot C_o + 1]}{s \cdot \frac{1}{2} \cdot [(2 \cdot R_c + R_o) \cdot C_o] + 1}$$

It should be apparent that analysis of switching converter feedback loops entails some algebra. Happily, after linearization the complete analysis is in the *s*-domain, familiar to electronics engineers. (See reference [22] for a more complete treatment.) When these final transfer blocks in the diagram of Fig. 7 are determined, we then have all the poles and zeros in the voltage loop and can draw frequency-response (Bode) plots of magnitude and phase from them alone to assess closed-loop gain magnitude and phase.

If the loop-gain phase angle is too high, the response is too underdamped and will ring excessively, causing voltages to deviate from the chosen design tolerance for output voltage. The poles and zero of Fig. 6, U6B are then adjusted in value to relocate them to where the resulting voltage-loop gain is sufficiently damped.

After adjusting damping, which might also reduce the low-frequency loop gain, making the steady-state accuracy insufficient, gain magnitude might need to be increased. If C3 of Fig. 6 is decreased, low-frequency gain and f_{p0} increase. Optimization of low-frequency gain (f_{p0}) and pole-zero placement is an exercise in control theory.

What has been glossed over here are the dynamics of the inner peak-current control loop. It consists of the CA power-transfer and current-sense circuits of Fig. 2, the PWM comparator (U5B, Fig. 6) and the control logic that drives the power switches, completing the loop. Reference [22] has an entire chapter and *How2Power Today* an entire article series posted on the home page on this topic.[23] It is not simple; in over six decades of refinement, four generations of models for it have been devised. The fourth-generation model (explained in the *H2P* series) has yet to diffuse widely and the second-generation model is still being promulgated.

Skill in feedback control design is required here, though hopefully this outline of what is involved will either enlighten you as a reader about how to proceed or sink your spirit if not mathematically inclined. If you are not mathematical, there still might be hope. I have encountered a few engineers who are comfortable with no higher math than arithmetic yet have an *intuitive qualitative* understanding for doing this kind of circuit design. Like Thomas Edison, they emphasize work at the bench (experiment) instead of desk (theory). It is possible to experiment with values for R21, C10, and C3 in Fig. 6 to develop a sense of how they affect loop dynamics.

However, math is a powerful tool, and when understood can be a faster, more optimal, and more insightful route to a satisfactory design. I have found that a dominant amount of desk-work followed by bench-work refinement is an optimal way to design. Both are necessary in that theoretical models of real circuits always fall short in some detailed ways discovered at the bench. When accounted for theoretically, theoretical models become more complete and desk-work more profitable. As an engineer grows in competence and experience, the desk-to-bench ratio increases because so much more that needs to be taken into account in a design is known beforehand.

References

1. "Designing An Open-Source Power Inverter (Part 1): Goals And Specifications" by Dennis Feucht, How2Power Today, May 2021.
2. "Designing An Open-Source Power Inverter (Part 2): Waveshape Selection" by Dennis Feucht, How2Power Today, September 2021.
3. "Designing An Open-Source Power Inverter (Part 3): Power-Transfer Circuit Options" by Dennis Feucht, How2Power Today, April 2022.
4. "Designing An Open-Source Power Inverter (Part 4): The Optimal Power-Line Waveshape" by Dennis Feucht, How2Power Today, May 2022.
5. "Designing An Open-Source Power Inverter (Part 5): Kilowatt Inverter Circuit Design" by Dennis Feucht, How2Power Today, July 2022.
6. "Designing An Open-Source Power Inverter (Part 6): Kilowatt Inverter Control Circuits" by Dennis Feucht, How2Power Today, August 2022.
7. "Designing An Open-Source Power Inverter (Part 7): Kilowatt Inverter Magnetics" by Dennis Feucht, How2Power Today, September 2022.
8. "Designing An Open-Source Power Inverter (Part 8): Converter Control Power Supply" by Dennis Feucht, How2Power Today, November 2022.
9. "Designing An Open-Source Power Inverter (Part 9): Magnetics For The Converter Control Power Supply" by Dennis Feucht, How2Power Today, December 2022.
10. "Designing An Open-Source Power Inverter (Part 10): Converter Protection Circuits" by Dennis Feucht, How2Power Today, February 2023.
11. "Designing An Open-Source Power Inverter (Part 11): Minimizing Switch Loss In Low-Input-Resistance Converters" by Dennis Feucht, How2Power Today, March 2023.
12. "Designing An Open-Source Power Inverter (Part 12): Sizing The Converter Magnetics" by Dennis Feucht, How2Power Today, May 2023.
13. "Designing An Open-Source Power Inverter (Part 13): The Differential Boost Push-Pull Power-Transfer Circuit" by Dennis Feucht, How2Power Today, June 2023.
14. "Designing An Open-Source Power Inverter (Part 14): Boost Push-Pull Or Buck Bridge?" by Dennis Feucht, How2Power Today, July 2023
15. "Designing An Open-Source Power Inverter (Part 15): Transformer Magnetic Design For the Battery Converter" by Dennis Feucht, How2Power Today, March 2024.
16. "Designing An Open-Source Power Inverter (Part 16): Transformer Winding Design For the Battery Converter—Efficiency Range And Winding Allotment" by Dennis Feucht, How2Power Today, April 2024.
17. "Designing An Open-Source Power Inverter (Part 17): Transformer Winding Design For the Battery Converter—Alternative Configurations" by Dennis Feucht, How2Power Today, May 2024.
18. "Designing An Open-Source Power Inverter (Part 18): Transformer Winding Design For The Battery Converter—Secondary Winding Design" by Dennis Feucht, How2Power Today, July 2024.
19. "Designing An Open-Source Power Inverter (Part 19): Controller Design For The Battery Converter" by Dennis Feucht, How2Power Today, September 2024.
20. "Designing An Open-Source Power Inverter (Part 20): Converter Inductor Magnetic Design" by Dennis Feucht, How2Power Today, October 2024.
21. "Designing An Open-Source Power Inverter (Part 21): Converter Inductor Winding Design" by Dennis Feucht, How2Power Today, November 2024.
22. *Power Converter Design Optimization* by Dennis Feucht, Innovatia (innovatia.com), covers details.
23. "Special Series On Current-Mode Control" by Dennis Feucht, How2Power.com.

About The Author

Dennis Feucht has been involved in power electronics for 40 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.

For further reading on power supply control topics, see the How2Power Design Guide, locate the Design Area category and select "Control Methods".