Current Mode-Controlled DC-DC Regulators (Part 2): Loop Compensation And Load Transient Performance

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Moving forward with the discussion of current-mode control, this article, part 2 of a multipart series, examines loop compensation of current-mode dc-dc regulators. Previously, part 1 reviewed the small-signal behavior of the inner current loop and outer voltage loop, including considerations for slope compensation, and presented the control-to-output transfer function for a buck regulator.[1]

The goal in the second installment of this series is to uncover simple expressions derived from the small-signal model to yield an intuitive compensator design procedure applicable to single- and multiphase regulator circuits. The simplicity of the design procedure, even with an error amplifier of finite gain bandwidth, will make it convenient for everyday use.

A design example using a commercially available two-phase synchronous buck controller, along with circuit simulation in the time and frequency domains, will substantiate the theoretical analysis and demonstrate how to select values for the compensation network to achieve a target crossover frequency. The simulations will then reveal how a lower compensation capacitance helps reduce the output voltage settling time following a load current transient.

Block Diagram

To recap part 1, Fig. 1 shows the block diagram model of a current-mode regulator with the outer voltage regulation loop closed. Transfer function $G_C(s)$ defines the compensator and includes the feedback resistor-divider network for output voltage sensing. Breaking the outer loop and injecting a signal between the regulator output node and upper feedback resistor enables measurement of the loop gain using techniques well established in engineering practice.

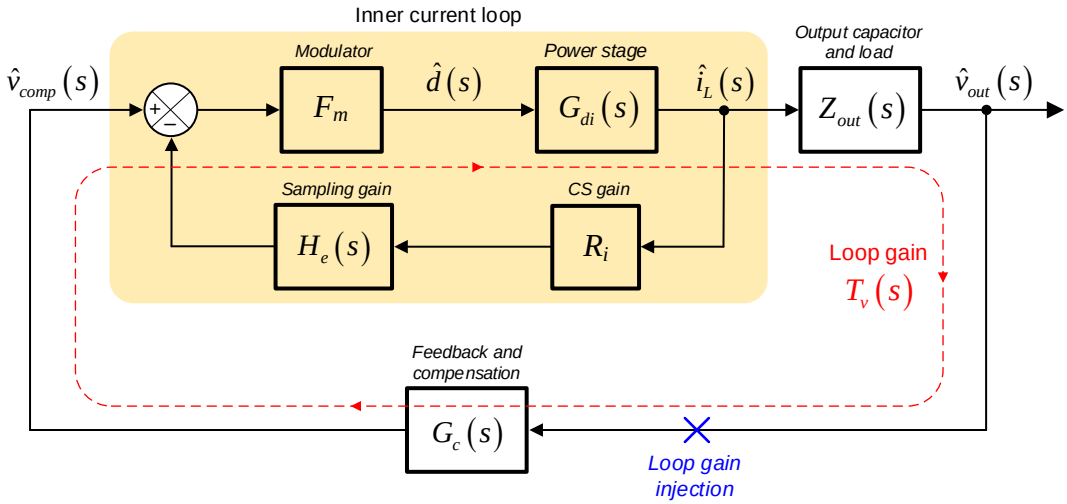

Fig. 1. Block diagram based on Ridley's sampled-loop model highlighting the loop gain, $T_v(s)$. $H_e(s)$ describes the sampling gain placed in the current-loop feedback path, as outlined in part 1 of this series.

In contrast, measurement of the inner current loop (shaded in Fig. 1) is normally unnecessary, although it is insightful to simulate it in order to appreciate the phenomenon at play with regard to selection of the slope compensation ramp, as you will see in the design example later.

Compensator Transfer Function

Fig. 2 shows how the outer voltage loop employs a conventional type-2 compensation circuit[2] using an error amplifier (EA) with output node labeled as COMP (short for "compensation" node). The amplifier model has transconductance g_m, output resistance R_{oEA} and effective bandwidth-limiting capacitance C_{bw}. The amplifier inverting input is the feedback (FB) node and connects to feedback resistors R_{fb1} and R_{fb2}.

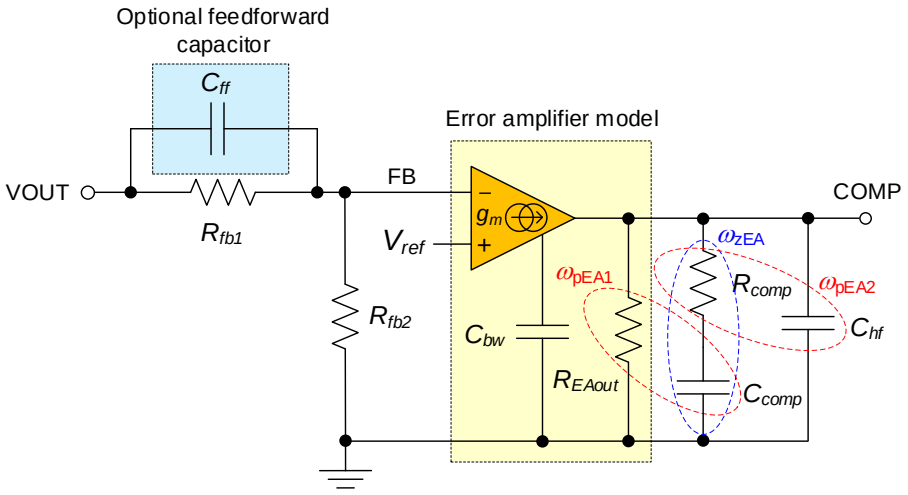

Fig. 2. Voltage-loop error amplifier with compensation network. The component combinations circled represent two poles and one zero.

As indicated in Fig. 2, R_{EAout} and C_{bw} set the dominant pole of the open-loop gain curve. You can express the open-loop gain of the amplifier as

$$G_{EA(\text{open loop})}(s) = -\frac{g_m R_{EAout}}{1 + sR_{EAout}C_{bw}} \qquad (1)$$

Equation 1 neglects any influence from high-frequency poles, whether parasitic or included by design. The compensator transfer function from VOUT to COMP, including the gain contribution A_{fb} from the feedback divider network, is

$$G_c(s) = \frac{\hat{v}_{comp}(s)}{\hat{v}_{out}(s)} = \frac{\hat{v}_{fb}(s)}{\hat{v}_{out}(s)}\frac{\hat{v}_{comp}(s)}{\hat{v}_{fb}(s)} = -A_{fb}(s)\,g_m Z_{EAout}(s) \qquad (2)$$

where the output impedance from Fig. 2 is

$$Z_{EAout}(s) = R_{EAout} \left\| \left(R_{comp} + \frac{1}{sC_{comp}} \right) \right\| \frac{1}{sC_{hf}} \left\| \frac{1}{sC_{bw}} \right. \qquad (3)$$

and the feedback attenuation factor is a constant based on the feedback divider ratio:

$$A_{fb} = \frac{\hat{v}_{fb}(s)}{\hat{v}_{out}(s)} = \frac{R_{fb2}}{R_{fb1} + R_{fb2}} \qquad (4)$$

If feedforward capacitor C_{ff} connects across R_{fb1}, a pole and a zero will appear that enable additional phase lead before crossover and unity gain at high frequency. The feedback gain then becomes

$$A_{fb}(s) = \frac{R_{fb2}}{R_{fb1}+R_{fb2}} \frac{1+sR_{fb1}C_{ff}}{1+s\left(R_{fb1}\|R_{fb2}\right)C_{ff}} \tag{5}$$

If ω_{pEA1} and ω_{pEA2} are well separated in frequency, the low-Q approximation applies and equation 3 becomes

$$Z_{EAout}(s) = R_{EAout} \frac{1+\frac{s}{\omega_{zEA}}}{\left(1+\frac{s}{\omega_{pEA1}}\right)\left(1+\frac{s}{\omega_{pEA2}}\right)} \tag{6}$$

where the frequencies are

$$\omega_{zEA} = \frac{1}{R_{comp}C_{comp}}$$

$$\omega_{pEA1} = \frac{1}{\left(R_{EAout}+R_{comp}\right)\left(C_{comp}+C_{hf}+C_{bw}\right)} \approx \frac{1}{R_{EAout}C_{comp}} \tag{7}$$

$$\omega_{pEA2} = \frac{1}{R_{comp}\left(C_{comp}\|\left(C_{hf}+C_{bw}\right)\right)} \approx \frac{1}{R_{comp}\left(C_{hf}+C_{bw}\right)}$$

As $R_{EAout} >> R_{comp}$ and $C_{comp} >> C_{hf}+C_{bw}$, the approximations set forth above are valid.

Circled in Fig. 2 (repeated below) are the components to provide two poles and one zero from the compensator. With × and o symbols denoting the respective pole and zero locations and a + symbol indicating the open-loop EA bandwidth, Fig. 3 gives a typical frequency response for the open-loop amplifier and the compensator. In this example, the feedback attenuation is set to unity, and the EA has an open-loop dc gain of 93 dB and a gain bandwidth of 13 MHz. Not included in the phase plots is the 180° phase shift related to the inverting amplifier configuration.

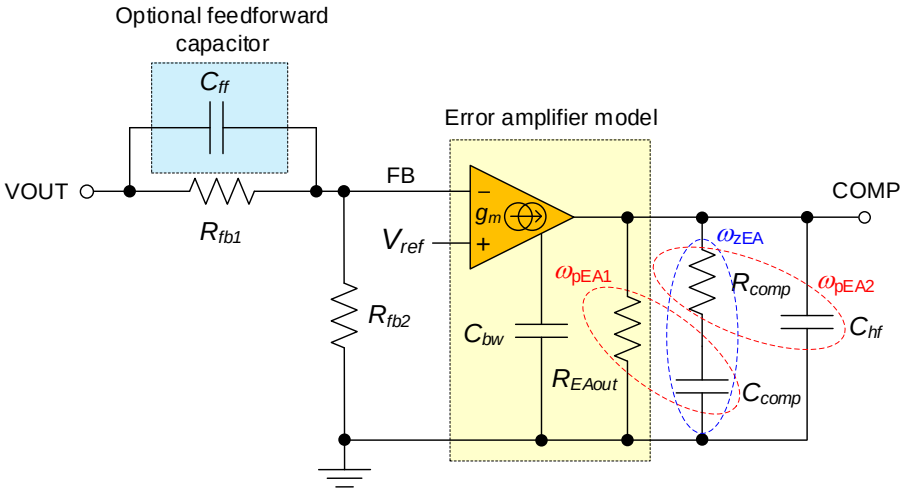

Fig. 2 (again). Voltage-loop error amplifier with compensation network. The component combinations circled represent two poles and one zero.

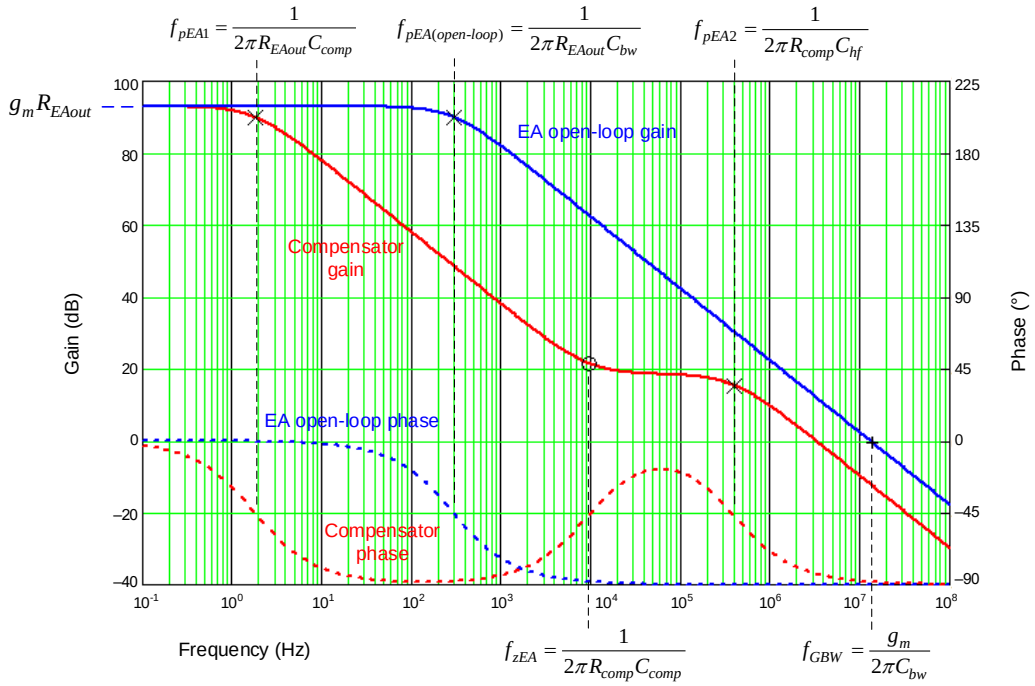

Fig. 3. Small-signal frequency responses of the open-loop EA and compensator with pole and zero frequencies indicated.

Compensator pole ω_{pEA1} appears at a very low frequency and is easily replaced by an integrator term. The compensator transfer function simplifies to

$$G_c(s) = -\frac{A_c}{s}\frac{1+\frac{s}{\omega_{zEA}}}{1+\frac{s}{\omega_{pEA}}} \qquad (8)$$

where A_c is the integrator gain term given by

$$A_c = \frac{g_m}{C_{comp}} A_{fb} \qquad (9)$$

Both feedback resistors, R_{fb1} and R_{fb2}, factor into the gain with a transconductance type EA. In contrast, the FB node with an op-amp-type EA is effectively at ac ground, and the lower feedback resistance has no influence on the loop dynamics.

Compensator Design

A frequently used compensation strategy that generally applies to peak, valley and emulated current-mode circuits is to equate the COMP-to-VOUT transfer function to the compensator transfer function term by term to attain a single-pole (–20 dB/decade) rolloff of the loop response. To demonstrate, consider:

- One compensator pole, ω_{pEA1}, positioned to provide high gain in the low-frequency range, minimizing the steady-state error of the output voltage.
- One compensator zero located to offset the load pole, $\omega_{zEA} > \omega_p$, using the typical minimum load resistance (maximum load current) condition.

- One compensator pole positioned to cancel the output capacitor equivalent series resistance (ESR) zero, $\omega_{pEA2} = \omega_{esr}$. Alternatively, if the ESR zero is at high frequency (with ceramic-only output capacitance), the compensator pole may locate at the switching frequency to reduce the switching ripple on the COMP voltage.

The loop gain is the product of the VOUT-to-COMP (compensator) and COMP-to-VOUT (control-to-output) transfer functions. Using equation 5 from part 1 and equation 7 above, the loop gain becomes:

$$T_v(s) = G_c(s)G_{c\text{-}o}(s) = -A_c A_{dc} \frac{1+\frac{s}{\omega_{zEA}}}{s\left(1+\frac{s}{\omega_{pEA}}\right)} \frac{1+\frac{s}{\omega_{esr}}}{\left(1+\frac{s}{\omega_p}\right)\left(1+\frac{s}{Q\omega_n}+\frac{s^2}{\omega_n^2}\right)} \qquad (10)$$

Select the crossover frequency $\omega_c = 2\pi f_c$ (where the loop gain is 0 dB) below a maximum 20% of the switching frequency. In practice, given the variation of ceramic output capacitance with temperature,[3] 10% to 15% of the switching frequency is an appropriate target for the crossover.

If $\omega_{zEA} = \omega_p$ and $\omega_{pEA} = \omega_{esr}$, the loop gain reduces to

$$T_v(s) \approx -\frac{A_c A_{dc}}{s} \frac{1}{1+\frac{s}{Q\omega_n}+\frac{s^2}{\omega_n^2}} \qquad (11)$$

Assuming a well-designed current loop with the amplitude of slope compensation[1] giving $0.5 \le Q \le 1$, the contribution from the sampling gain (a double pole at half switching frequency) is insignificant at frequencies up to the crossover. Of course, this assumption precludes the case where the slope-compensation amplitude is high and the resultant value of Q is low, thus imparting additional phase lag at crossover.

The magnitude of the loop gain at the dominant pole frequency is

$$\left|T_v\left(j\omega_p\right)\right| = \left|T_v\left(j\omega_{zEA}\right)\right| \approx A_c A_{dc} R_{comp} C_{comp} = g_m A_{FB} A_{dc} R_{comp} \qquad (12)$$

It is evident, using basic Bode plot principles, that

$$\left|T_v\left(j\omega_p\right)\right| \approx \frac{\omega_c}{\omega_p} \qquad (13)$$

and then a straightforward expression for the crossover frequency is

$$f_c = f_p g_m A_{fb} A_{dc} R_{comp} \qquad (14)$$

Finally, you can calculate compensation component values sequentially as

$$R_{comp} = \frac{1}{g_m A_{fb} A_{dc}} \frac{f_c}{f_p}, \qquad C_{comp} = \frac{5}{\omega_c R_{comp}}, \qquad C_{hf} = \frac{1}{\omega_{esr} R_{comp}} - C_{bw} \qquad (15)$$

where R_{comp} is proportional to the crossover frequency and C_{comp} sets the phase margin. You will find a value for the compensation capacitance to locate the zero at one-fifth the target crossover frequency, which normally results in adequate phase boost at crossover.

Choosing a value for the lower feedback resistor gives the upper feedback resistance as

$$R_{fb1} = R_{fb2}\left(\frac{V_{out}}{V_{ref}} - 1\right) \qquad (16)$$

Note that the compensation zero represents the dominant time constant that significantly affects the settling time of the output voltage following a load transient. An unnecessarily high value for C_{comp} thus runs counter to an objective for a fast settling time. As such, you can adjust C_{comp} to optimize the settling time while still maintaining a phase margin in a window of 50° to 60°.

Design Example

Taking a specific example to illustrate the component selection process, the following table specifies the circuit operating conditions, power-stage component values and control circuit parameters of a buck regulator using the LM5137F-Q1 peak current-mode controller[3] from Texas Instruments (TI). The design operates in an interleaved two-phase configuration with a switching frequency of 400 kHz and converts from a nominal input voltage of 48 V to an output voltage of 12 V.

Table. Power-stage and controller parameters for a two-phase buck regulator design.

Power-stage parameters				**Controller parameters**			
$V_{in(nom)}$	48 V	L_o	4.7 µH	G_i	10	$S_{n\text{-}internal}$	306 mV/µs
V_{out}	12 V	R_{dcr}	8.3 mΩ	R_i	40 mΩ	$S_{f\text{-}internal}$	102 mV/µs
I_{out}	20 A	C_o	90 µF	g_m	600 µS	$S_{e\text{-}internal}$	84 mV/µs
No. of phases	2	R_{esr}	2 mΩ	R_{EAout}	74 MΩ	m_c	1.275
f_s	400 kHz	R_s	4 mΩ	C_{bw}	7.3 pF	Q	0.7

The buck inductance and current-sense resistance given in the table are already per-phase values. However, the values for load resistance and output capacitance correspond to the total for the two-phase configuration, and translating to a per-phase equivalent circuit requires twice-resistance and half-capacitance values, as expected. In practice, only one parameter in the loop-gain expression requires adjustment for the multiphase circuit: the load resistance scales by the number of phases in the expressions to calculate A_{dc}.

Updating equation 16 in part 1, the expressions for a multiphase design become

$$k_d = 1 + \frac{N_p R_{load} T_s}{L_o}\left(m_c D' - 0.5\right), \qquad A_{dc} = \frac{N_p R_{load}}{R_i}\frac{1}{k_d} \qquad (17)$$

where N_p is the number of phases.

Given a duty cycle of 25% for this design example, the calculation of A_{dc} is

$$k_d = 1 + \frac{N_p R_{load} T_s}{L_o}\left(m_c D' - 0.5\right)$$
$$= 1 + \frac{2 \times 0.6\Omega \times 2.5\mu s}{4.7\mu H}\left(1.274 \times 0.75 - 0.5\right) = 1.26 \qquad (18)$$
$$A_{dc} = \frac{N_p R_{load}}{R_i}\frac{1}{k_d} = \frac{2 \times 0.6\Omega}{40\,m\Omega}\frac{1}{1.26} = 23.8$$

A voltage derating of capacitance is now necessary if the output capacitors have ceramic dielectric. Given that a Murata 22-µF, 25-V, 1210 X7R ceramic capacitor is effectively 9 µF at 12 V and room temperature,[4] an approximate derating to 40% of the nameplate value (10 capacitors at 9 µF each) applies in these calculations. The frequencies for the load pole and ESR zero are

$$f_p = \frac{k_d}{2\pi R_{load} C_o} = \frac{1.26}{2\pi \times 0.6\Omega \times 90\mu F} = 3.72\,kHz$$
$$f_{esr} = \frac{1}{2\pi R_{esr} C_o} = \frac{1}{2\pi \times 2\,m\Omega \times 90\mu F} = 884\,kHz \qquad (19)$$

Given a target crossover frequency of 50 kHz, calculate the compensation component values using expressions from equation 15. As the ESR zero frequency is relatively high at 884 kHz, you can instead place the compensator high-frequency pole at the switching frequency for noise attenuation.

$$R_{comp} = \frac{1}{g_m A_{fb} A_{dc}}\frac{f_c}{f_p} = \frac{1}{0.6\,mS \times \frac{0.8\,V}{12\,V} \times 23.8} \times \frac{50\,kHz}{3.72\,kHz} = 14\,k\Omega$$
$$C_{comp} = \frac{5}{\omega_c R_{comp}} = \frac{5}{2\pi \times 50\,kHz \times 14\,k\Omega} = 1.2\,nF \qquad (20)$$
$$C_{hf} = \frac{1}{\omega_s R_{comp}} - C_{bw} = \frac{1}{2\pi \times 400\,kHz \times 14\,k\Omega} - 7.3\,pF = 22\,pF$$

Selecting standard E96 resistor values of 93.1 kΩ and 6.65 kΩ for the feedback divider yields an output voltage setpoint of exactly 12 V.

$$V_{out} = V_{ref}\left(1 + \frac{R_{fb1}}{R_{fb2}}\right) = 0.8V \times \left(1 + \frac{93.1k\Omega}{6.65k\Omega}\right) = 12V \qquad (21)$$

Fig. 4 shows Mathcad-derived loop gain and phase plots for this example. The phase margin (PM or ϕ_M) is the difference between the phase at crossover and −180° (EA inversion phase-lag contribution not included). The COMP-to-VOUT transfer function is a three-pole system—the dominant load pole at 3.7 kHz and the double pole at half switching frequency related to the sampling gain. The compensator zero offsets the load pole while allowing a slight phase dip, as the zero is set at a higher frequency than the pole and is not an exact cancellation.

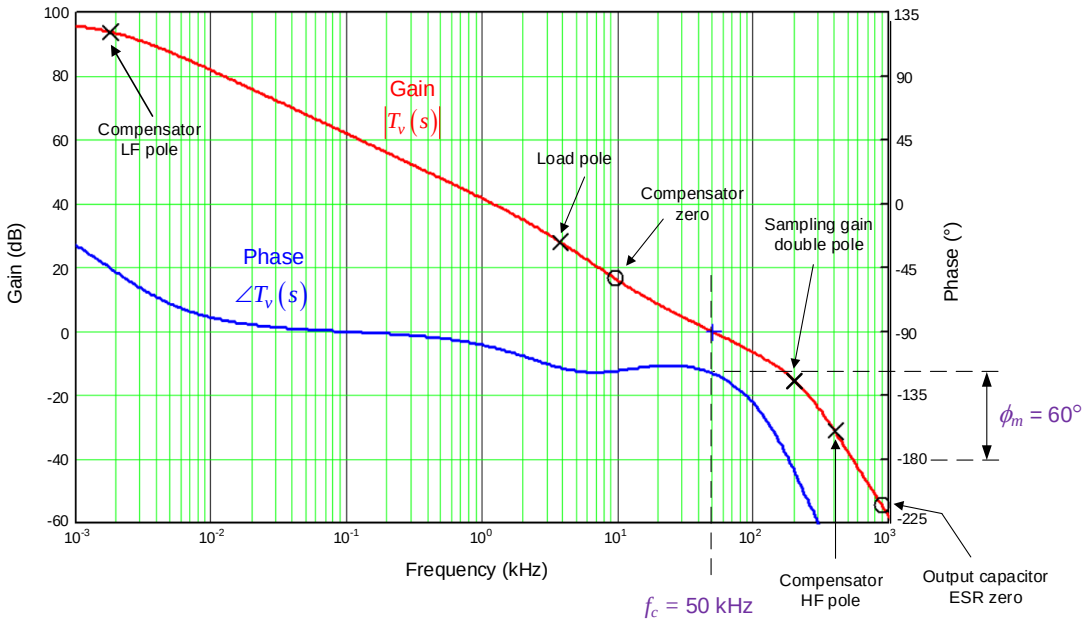

Fig. 4. Loop-gain magnitude and phase plots, accurate to half switching frequency.

Circuit Simulation

Using a two-phase synchronous buck controller in a regulator configuration defined by the parameters in the earlier table, Fig. 5 presents a SIMPLIS simulation schematic to confirm the analysis previously outlined. SIMPLIS enables easy generation of Bode plots without resorting to the average models that SPICE requires. As shown, you can measure the outer loop gain $T_V(s)$ by breaking the loop above the upper feedback resistor, injecting a variable frequency oscillator signal and analyzing the frequency response.

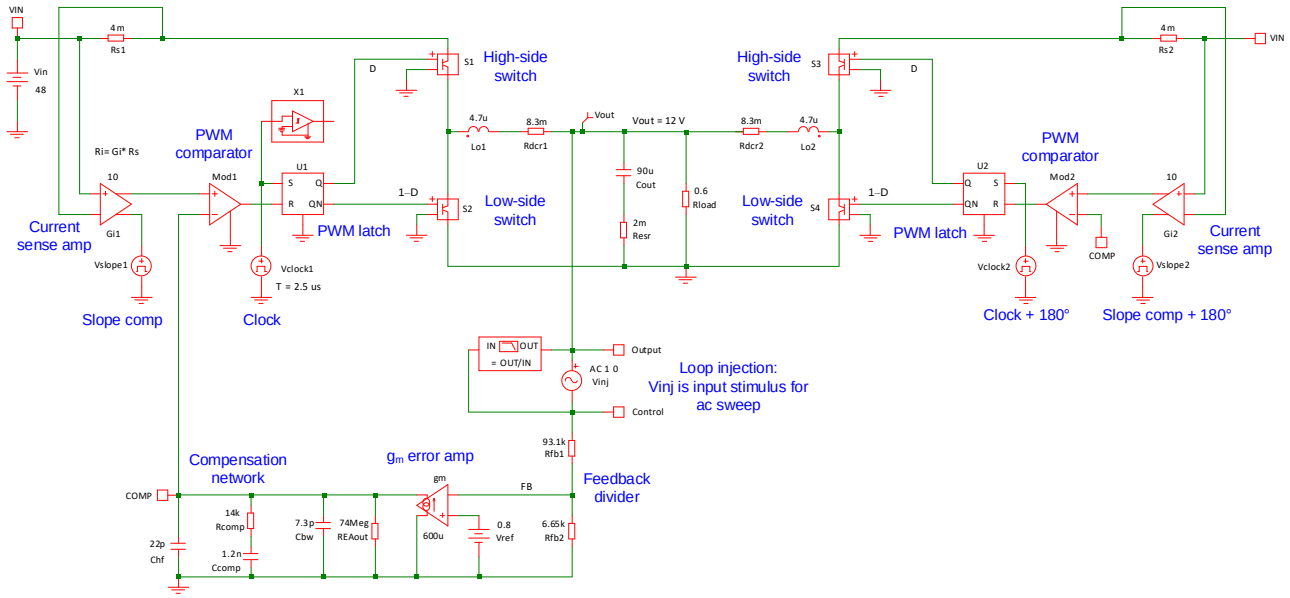

Fig. 5. SIMPLIS simulation schematic of a two-phase buck regulator (48 V to 12 V at 20 A).

The element with reference designator X1 in Fig. 5 (just above the PWM latch in the upper left of schematic) is the SIMPLIS clock edge trigger to find the periodic operating point (POP) of the circuit before running the

frequency- or time-domain analyses. The POP works on the full nonlinear switching time-domain model of the circuit and enables subsequent ac or transient simulations. The ac source with reference designator Vinj in Fig. 5 is the input stimulus for the ac sweep. Automatically controlling its amplitude in the simulation keeps the ac response in the linearized small-signal region.

First, check the stability of inner current loop gain $T_i(s)$. As outlined in part 1, the slope compensation ramp serves to reduce the overall gain of the current loop[1] and forces crossover at a more favorable point where phase margin improves.

To facilitate measurement of the current loop, a digital modulator SIMPLIS subcircuit developed and made available by Christophe Basso[5] connects at the output of the PWM latch and perturbs the duty cycle. With the COMP voltage adjusted to set the output to 12 V with a 1.2-Ω load resistance, Fig. 6 shows the Bode plot simulation results. The current loop is stable with a crossover of 70 kHz and a phase margin of 61°. This crossover is close to the theoretical 0-dB crossover pole, estimated with $H_e(s)$ = 1 and given by:

$$f_{po} \approx \frac{f_s}{2\pi m_c D'} = \frac{400\,\text{kHz}}{2\pi \times 1.274 \times 0.75} = 67\,\text{kHz} \qquad (22)$$

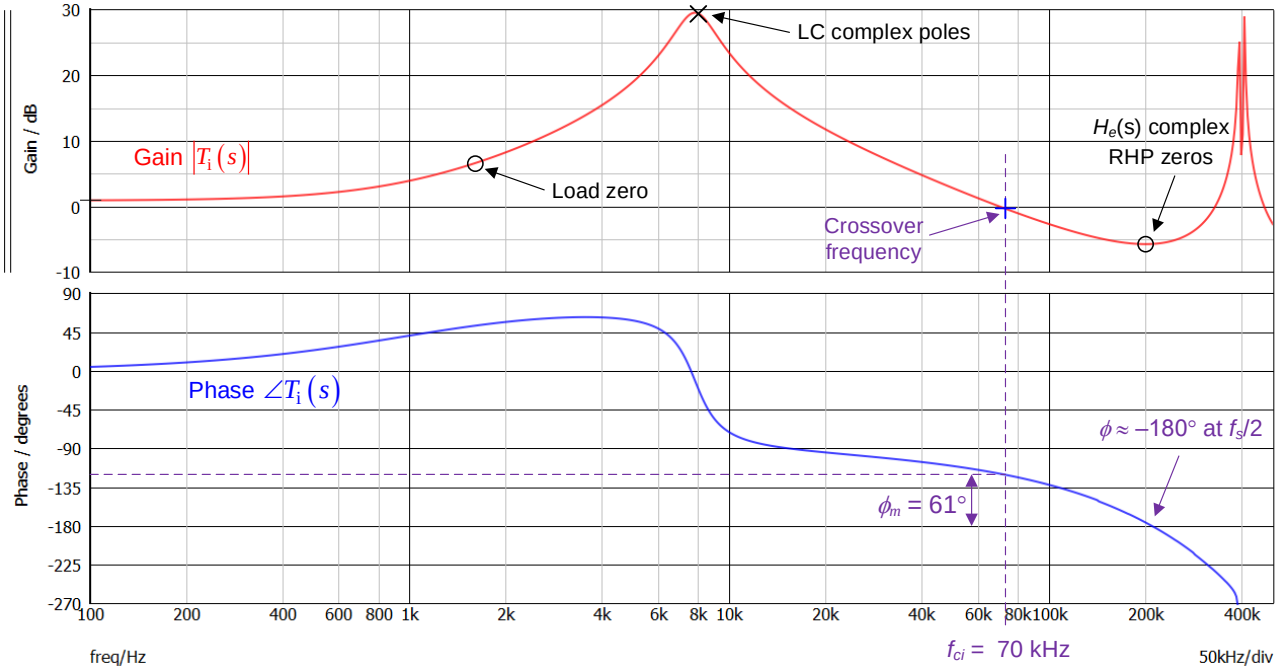

Fig. 6. Simulated current-loop gain (magnitude, phase) results with the voltage loop open.

Fig. 7 illustrates Bode plot simulation results for the outer voltage loop, where the solid and dotted lines correspond to two different values of compensation capacitances, 1.2 nF and 2.2 nF, which set the compensator zero at 9.5 kHz and 5.2 kHz, or approximately one-fifth and one-tenth the target crossover frequency, respectively. The solid line in Fig. 7 closely matches well with the analytical result in Fig. 4 up to half the switching frequency, as expected, with a crossover frequency of 50 kHz and a phase margin of 60°.

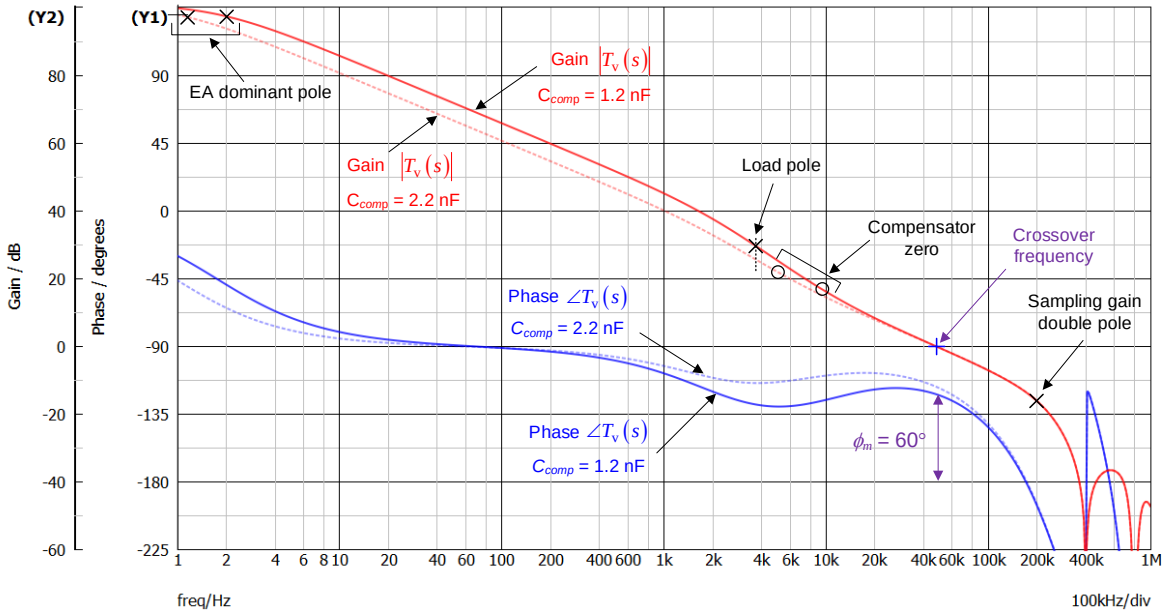

Fig. 7. Simulated voltage-loop gain (magnitude, phase) plots with two values of compensation capacitance, C_{comp}.

Using a time-domain analysis in SIMPLIS, Fig. 8 shows load-on and load-off transient responses for the two values of C_{comp}. The load step is from 50% to 100% of the rated load (10 A to 20 A) at a slew rate of 1 A/µs.

Clearly, the lower compensation capacitance gives a faster settling time of the output voltage, reduced from approximately 100 µs to 50 µs. Interestingly, this is achieved with very little change in the Bode plot: placing the compensator zero at the higher frequency only reduces the phase margin by 5°; as shown in Fig. 7. The crossover frequency stays constant, which is also evident in Fig. 8 since there is no change in the output-voltage peak deviation. A general rule of thumb to select C_{comp} is to set the time constant for $R_{comp}C_{comp}$ at about 20 µs.

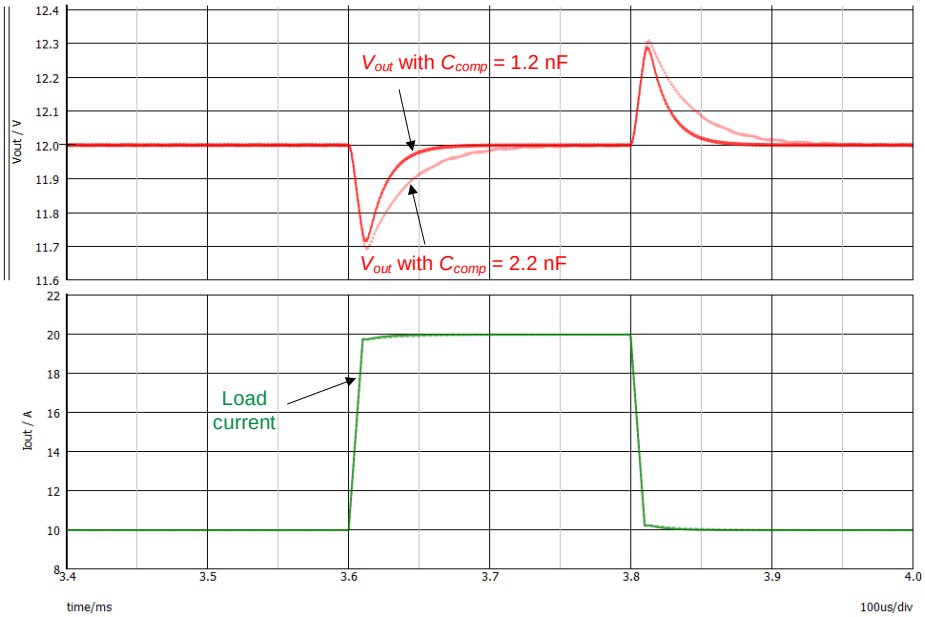

Fig. 8. Simulated 10-A load-step response with C_{comp} values of 1.2 nF and 2.2 nF.

Fig. 9 shows Bode plot simulations for the schematic of Fig. 5 with load resistances of 0.6 Ω, 1.2 Ω, 2.4 Ω and 4.8 Ω, corresponding to load currents of 20 A, 10 A, 5 A and 2.5 A, respectively. As shown in Fig. 9, as the load resistance increases, the load pole slides lower in frequency (from 3.7 kHz to 1.2 kHz) and the low-frequency gain increases, but the crossover frequency stays constant and the phase margin has only minimal change. These trends are also apparent from equations 18 and 19.

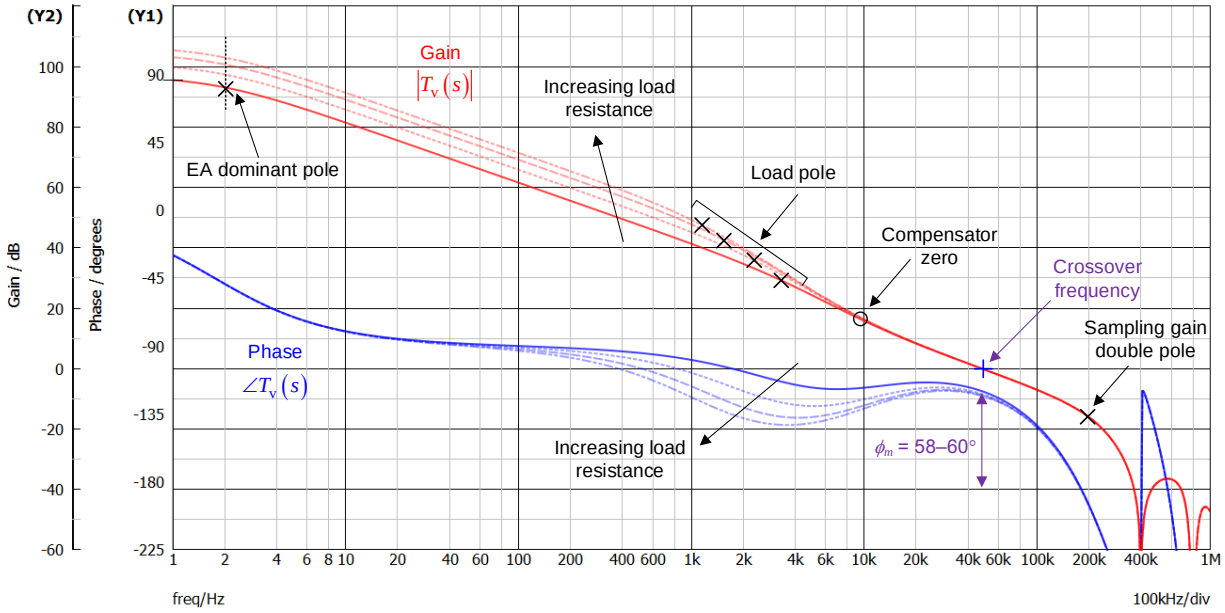

Fig. 9. Simulated voltage-loop gain (magnitude, phase) plots with varying load resistance.

Fig. 10 shows the same load transient measured experimentally with an equivalent hardware implementation using the TI LM5137F-Q1 two-phase buck controller evaluation module.[3] The output voltage behavior during both the rising and falling transients closely matches the simulated result of Fig. 8.

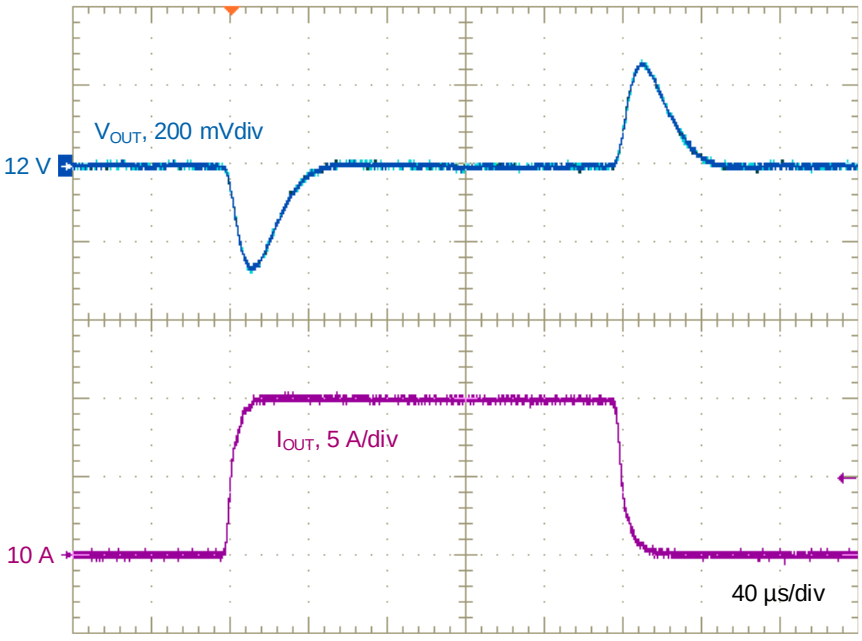

Fig. 10. Measured load transient response with the current slew rate (di/dt) = 1 A/µs.

Summary

The primary objective of this article was to present a simple procedure for loop compensation design of a current-mode buck regulator. The procedure uses the target crossover frequency as a starting point to derive values for the compensation network components. Suitable selection of the compensation capacitance optimizes the settling time of the load transient response while maintaining adequate phase margin.

Simulation results and practical circuit measurements confirm the analytical expressions. A design example for compensation of a two-phase buck regulator shows that the Bode plot and load transient response, whether obtained by simulation or bench measurement, go hand in hand while optimizing a dc-dc regulator. The two methods are complementary, although some designers will only measure the transient response as taking Bode plot measurements requires more effort.

The next installment in this series will discuss a novel constant-current, constant-voltage dual-loop architecture with a shared compensation network.

References

1. "Current Mode-Controlled DC-DC Regulators (Part 1): A Review of Small-Signal Behavior," by Timothy Hegarty, How2Power Today, November 2024.
2. "An Intuitive Guide to Compensating Switching Power Supplies," by Christophe Basso, Stairway Press, 2024.
3. LM5137F-Q1 synchronous buck controller evaluation module (12 V, 20 A, 400 kHz).
4. Murata Simsurfing web tool for ceramic capacitors.
5. SIMPLIS digital modulator subcircuit for current loop measurement, Christophe Basso.

About The Author

Timothy Hegarty is a senior member technical staff (SMTS) in the Switching Regulators business unit at Texas Instruments. With over 25 years of power-management engineering experience, he has written numerous conference papers, articles, seminars, white papers, application notes and blog posts. Tim's current focus is on enabling technologies for high-frequency, low-EMI, isolated and nonisolated regulators with a wide input-voltage range, targeting industrial, communications and automotive applications. He is a senior member of the IEEE and a member of the IEEE Power Electronics, Industrial Applications and EMC Societies.

For further reading on current mode control, see the "How2Power Design Guide," locate the Design Area category and select Control Methods.