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Designing An Open-Source Power Inverter (Part 23): Inverter Driver Design Refinement

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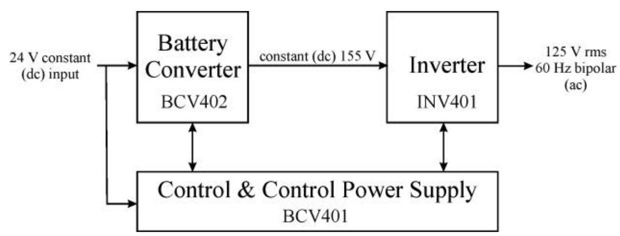
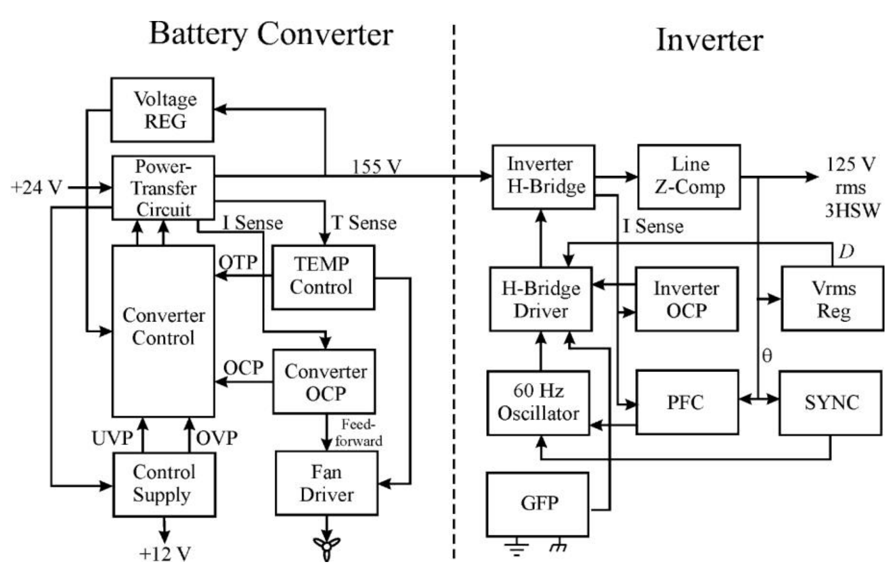
Experienced design engineers can anticipate almost all of what needs to be considered in a design project. More involved projects, such as the design of an oscilloscope for instrument engineers, are straightforward for perhaps 95% of the project before anomalous behavior is encountered on the bench. The final 5% of the project becomes a research effort to find causes for unanticipated problems that can absorb 50% of the time of the project. This is why in the 1960s at Tektronix, planners would multiply the project time resulting from careful estimation by two to devise a more realistic project schedule. The Volksinverter design is no exception, and refinement of the earlier design work discussed in previous parts is necessary.

In this latest installment in the Volksinverter series,[1-22] some further attention is given to the design of the inverter stage (Fig. 1). Specifically, we correct some errors in the H-bridge circuitry by making adjustments to the bypass capacitance, changing the off-biasing of the high-side driver for a better voltage margin, suggesting synchronization of battery converter and the inverter switching cycles to reduce ripple current, and fixing some problems with the gate-drive circuitry and the overcurrent protection (OCP) circuitry. Additionally, we clarify requirements for the ground-fault protection circuitry for larger inverter systems where common-mode currents pose a greater risk to inverter operators.



(a)



(b)

Fig. 1. The Volksinverter's system block diagram (a) and an expanded block diagram showing details of the inverter stage which will be discussed in this part (b).

H-Bridge Driver Design Problem

The INV401 H-bridge circuit from part 5[5] requires some refinement. An additional supply bypass capacitor C12 provides ripple current that would otherwise exceed the current rating of electrolytic capacitor C18. In addition, the converter switching cycle could be synchronized with the inverter PWM cycle to minimize *i*(C18) as in some PFC converters, though they operate at different frequencies. If the on-times of converter and inverter are concurrent, then C18 ripple current is minimized. Otherwise, converter and inverter waveforms are asynchronous, and calculation of *i*(C18) is not a simple task.

Q15 and Q11 base resistors R9 and R10 are reconnected directly to the collectors of Q13 and Q12 as shown in Fig. 2 so that the high-side MOSFET gate voltages are pulled low enough to keep the Q2 and Q6 off. They translate from the low-side gate driver output up to the high-side voltage.

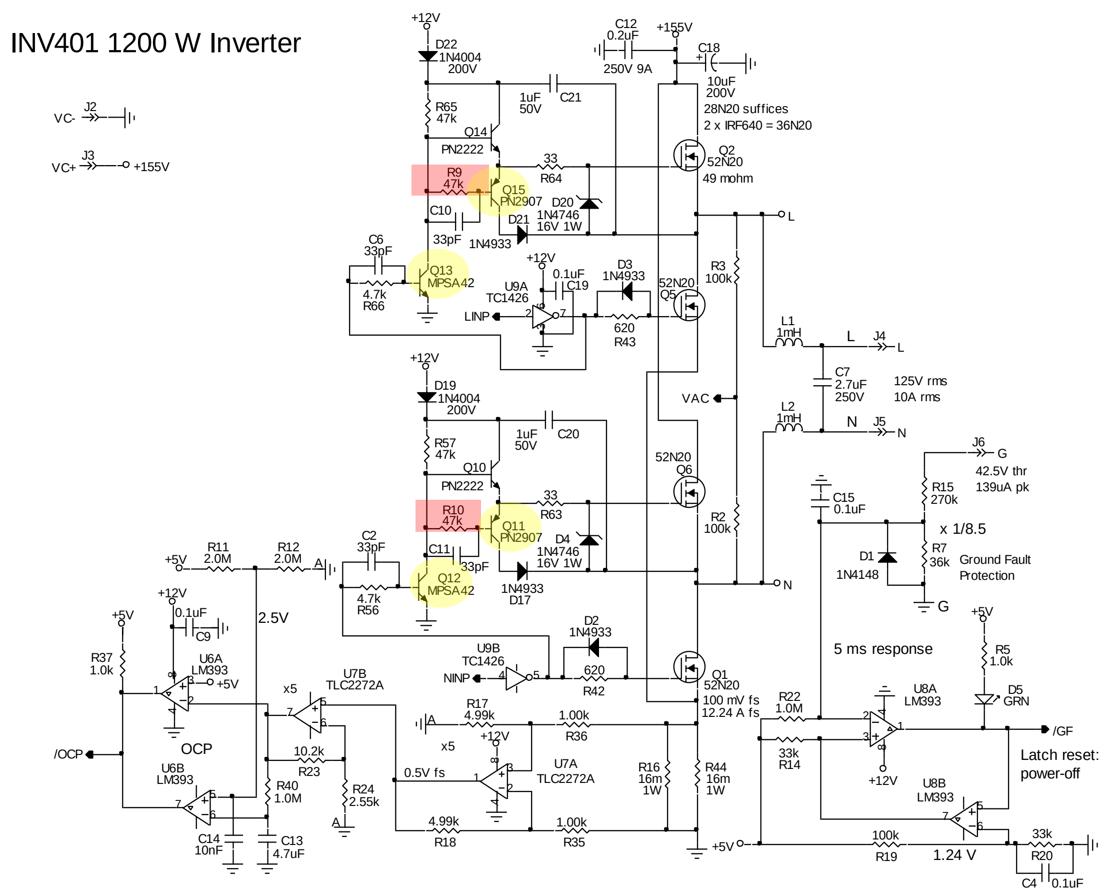


Fig. 2. Modified design of INV401 H-bridge drivers connect R9 and R10 directly to Q13 and Q12 collectors to be pulled down to ground when Q13 and Q12 are on. (The resistors mentioned here are highlighted in red, while transistors Q11, Q12, Q13 and Q15 are highlighted in yellow.)

The high-side gate drivers are designed with discrete BJTs though integrated high-side drivers could have been used instead. Q13 and Q12 translate from the low-side gate driver output up to the high-side voltage. When a U1 output goes low in the inverter control circuit,[6] Q13 or Q12 shut off and Q14 or Q10 conduct, charging the gate capacitance through R63 or R64. D20 or D4 are overvoltage protection of the MOSFET gate-source inputs for both polarities.

When the high-side MOSFET shuts off, charge is removed from C_{GS} by conduction of Q15 or Q11. D21 and D17 prevent forward-biasing of the Q15 and Q11 c-b junctions during a high output undergoing a high-to-low transition. Q13 and Q12 switch on to bring their half-bridge outputs low but while they are still high, a conduction path otherwise exists through Q15 and Q11 c-b junctions.

The cathodes of diodes D22 and D19 are at V_{GH} and are elevated above +155 V by the gate-supply voltage across C21 and C20. When the output of the half-bridge is low, C21 or C20 charge through D22 or D19 to a voltage of V_{GH} = 12 V – $V_D \approx$ 11.2 V. The 52N20 MOSFET gate charge over the total ΔV_G is specified as $Q_G \leq$ 200 nC; thus $C_G \leq$ 5 nF. The ripple voltage across C20 = C21 = 1 μF is ΔV_{GH} = (200 nC)/(1 μF) = 200 mV, resulting in an acceptable V_{GH} = 11.2 V – 0.2 V = 11 V.

The time-constant to switching on is $\tau_{on} \approx$ (33 Ω)·(5 nF) = 165 ns. Q12 and Q13 are MPSA42A having f_T = 50 MHz at 10 mA and $\beta_0 \approx$ 40. Q14 and Q10 are PN2222A with $\beta_0 + 1 \geq 100$. The on-time and off-time gate currents are

$$I_G(\text{on}) \approx \frac{10\ \text{V}}{47\ \text{k}\Omega}\cdot(100) = 21.3\ \text{mA} \Rightarrow$$

$$t_{sw}(\text{on}) \approx \frac{(10\ \text{V})\cdot(5\ \text{nF})}{21.3\ \text{mA}} = 2.35\ \mu\text{s}$$

$$I_G(\text{off}) \approx \frac{155\ \text{V}}{47\ \text{k}\Omega}\cdot(100) = (3.30\ \text{mA})\cdot(100) = 330\ \text{mA}$$

However, when switched off, Q11, R63 and D17, and Q15, R64 and D21 are the paths discharging gate-source capacitance, limited to a discharge current of

$$I_G \geq [V_{GS}(\text{on}) - V_D]/R_G = 9\ \text{V}/33\ \Omega = 0.27\ \text{A} \Rightarrow$$

$$t_{sw}(\text{off}) \leq (200\ \text{nC})/(0.27\ \text{A}) = 741\ \text{ns}$$

Thus t_{sw}(on) << t_{sw}(off) and there is no H-bridge shoot-through.

At the bottom of the H-bridge are two sense resistors R16 and R44 with a combined 8 mΩ driving the U7A diff-amp which drives the previous OCP circuit (at INP), now drawn correctly. The parasitic series inductance of R16 and R44 is minimized to avoid voltage spikes when the low-side power switches switch on. Inductance is minimized by using four-wire (Kelvin) resistors, with separate drive and sense terminal-pairs.

As given, the circuit design has no low-pass RC filter following the sense resistors but inputs directly to a one-op-amp differential amplifier (U7A). Differential sensing across the sense resistance minimizes added inductance from additional wire length.

R2 and R3 form a voltage divider for feeding back the output waveform (VAC) to detect zero-crossings to synchronize with the power-line waveform if present from other INV401 modules, to make them scalable.

In the next Volksinverter article, we face the worst design conundrum of the project, caused by not paying enough attention during inverter design to the output filter and EMI generation.

Volksinverter Ground-Fault Protection

The Volksinverter design does not isolate the converter and inverter stages; they share a common ground which is the battery-bank negative terminal. The third (green) wire that is the safety ground in electrical-power distribution is intended to bypass current from the line or "hot" terminal L to the neutral or N terminal when a fault shorts L to the metal enclosure of an appliance. The third wire is by design connected to N at the source.

The safety ground wire shorts the case to N, bypassing a user touching the case who would otherwise be holding the L terminal, and if grounded (to N) would be subjected to line voltage. Ground-fault interrupters are built into outlet receptacles to open the L terminal to the load if such a fault occurs.

In battery inverters, the functional equivalent of a ground-fault interrupter is included in the design. In the Volksinverter, the safety ground is connected to a *ground-fault protection* (GFP) circuit (see Fig. 3) that shuts down the inverter if the green-wire voltage relative to inverter ground exceeds a safe value according to UL in the 1970s of 42.5 V, based on the pre-48-V safety standard. (Humans since then must have evolved to safely sustain higher voltage!)

The L output terminal is connected to ground through the H-bridge during the negative output half-cycle and to V_c during the positive half-cycle. The Volksinverter GFP activates during the positive half-cycle.

The nominal 24 V (30 V max) battery input of the Volksinverter is below the unsafe value. The Volksinverter ground system is required to be isolated from extraneous connections (such as earth ground) with low parasitic common-mode current i_{CM} attenuated sufficiently by the output filter. Consequently, the converter is not isolated conductively from the inverter.

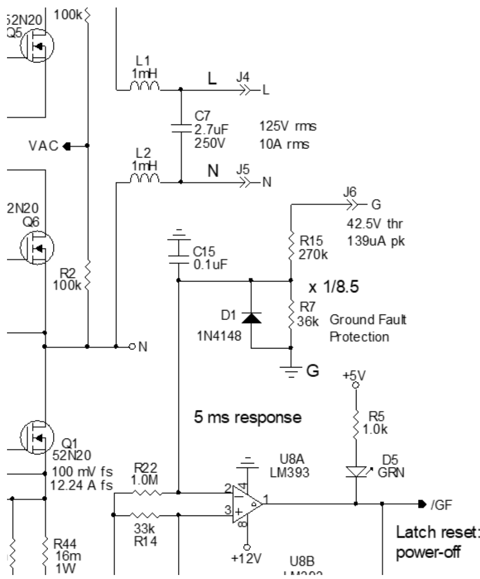


Fig. 3. A closeup of the GFP components in the inverter stage.

Commercial low-cost inverters under a kilowatt are typically not isolated either as are some higher-power transformerless inverters. However, in larger inverter systems (≥ 10 kW), neither extraneous connective paths or parasitic capacitive coupling through C_{CM} can be excluded and i_{CM} poses not only an overcurrent hazard to inverter power switches but also to anyone connected between the two otherwise-isolated systems.

Consequently, for safety in such higher-power systems, the converter and all input components, including solar charger, battery-banks and PV array, are conductively isolated from the inverter stage so that no extraneous conductive paths back to the converter side of the system exist from the inverter output terminals, reducing i_{CM} to what conducts through parasitic C_{CM}.

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Dennis Feucht has been involved in power electronics for 40 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.

For further reading on power supply control topics, see the How2Power Design Guide, locate the Design Area category and select "Control Methods".